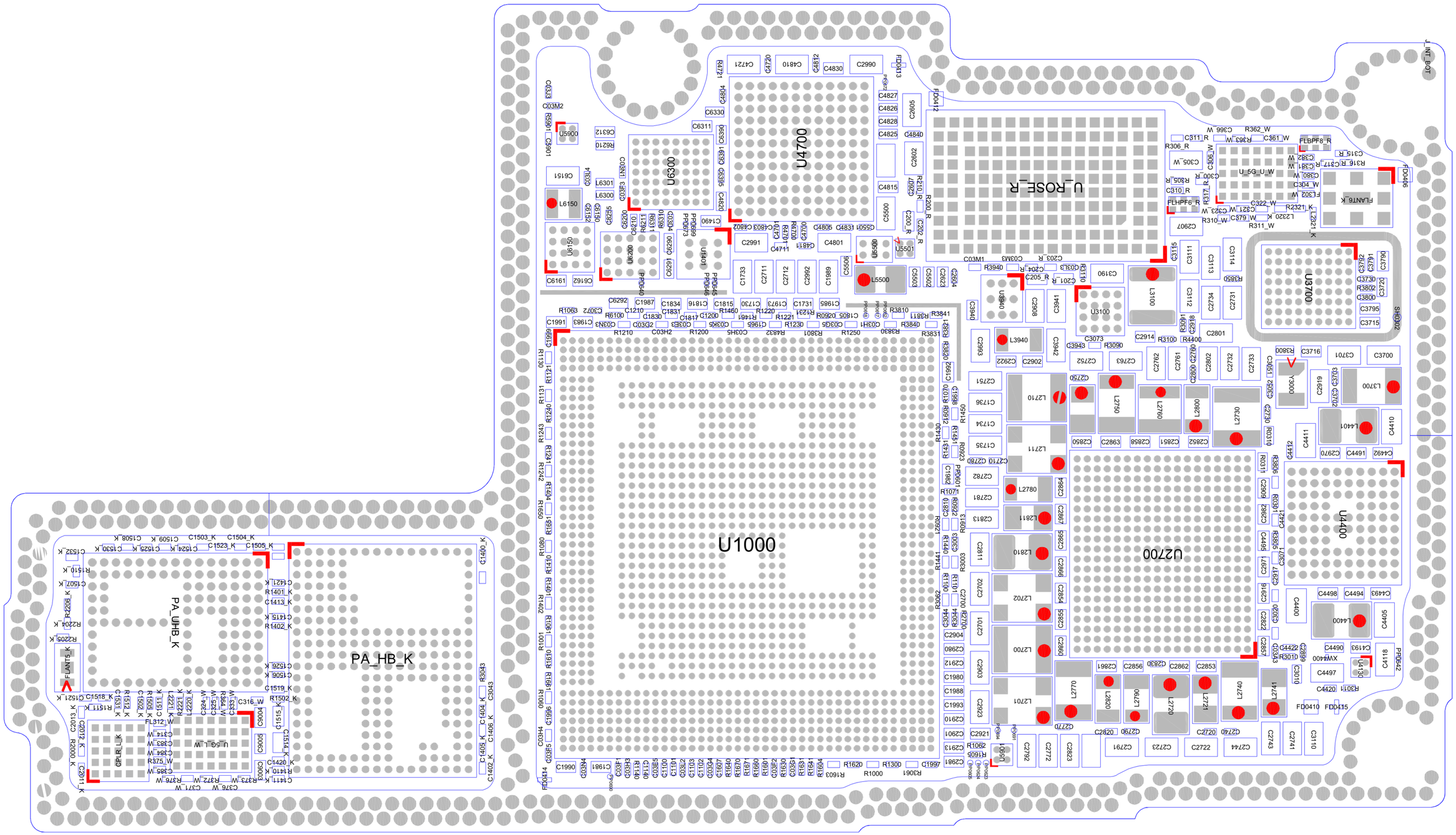
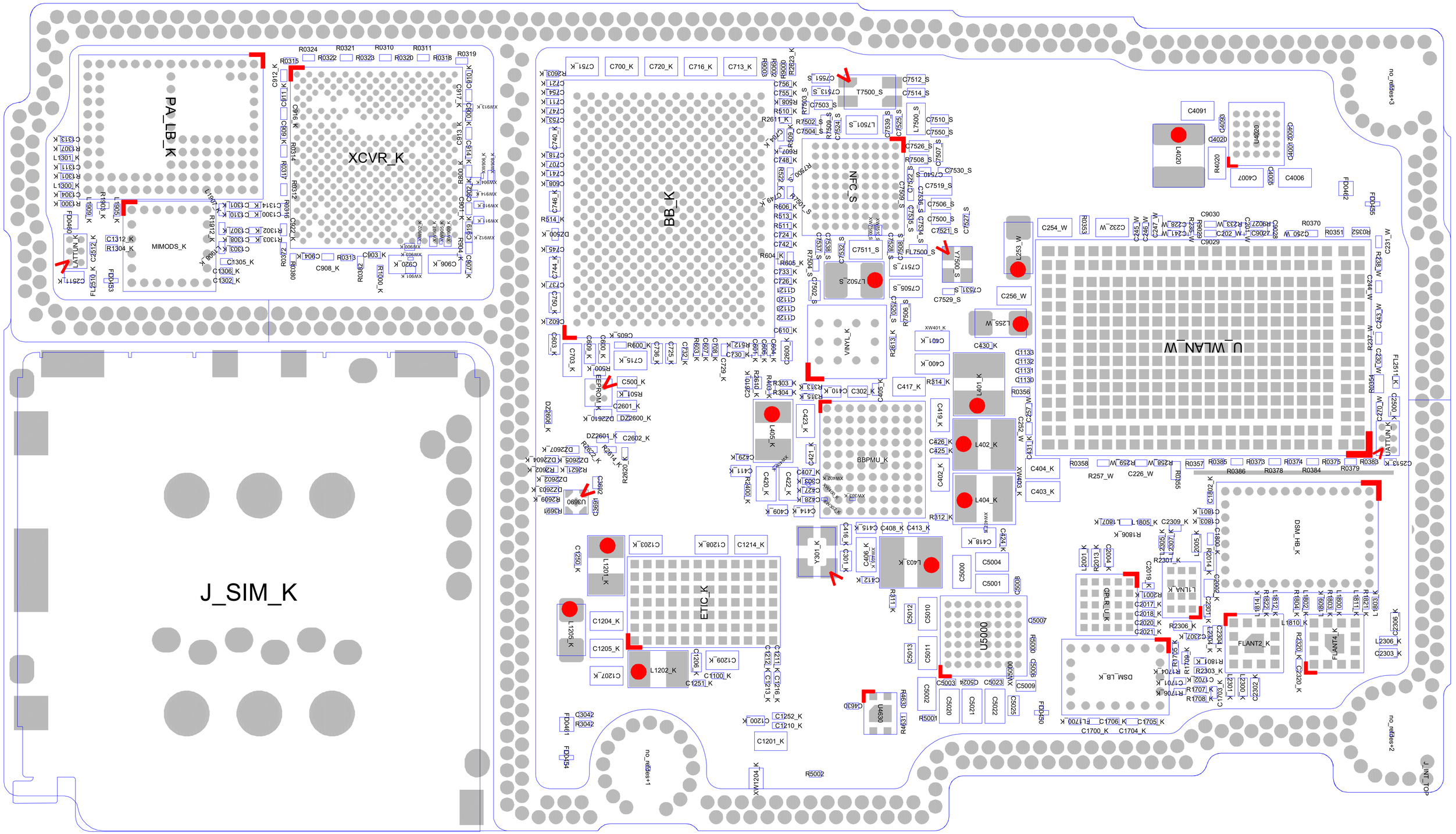
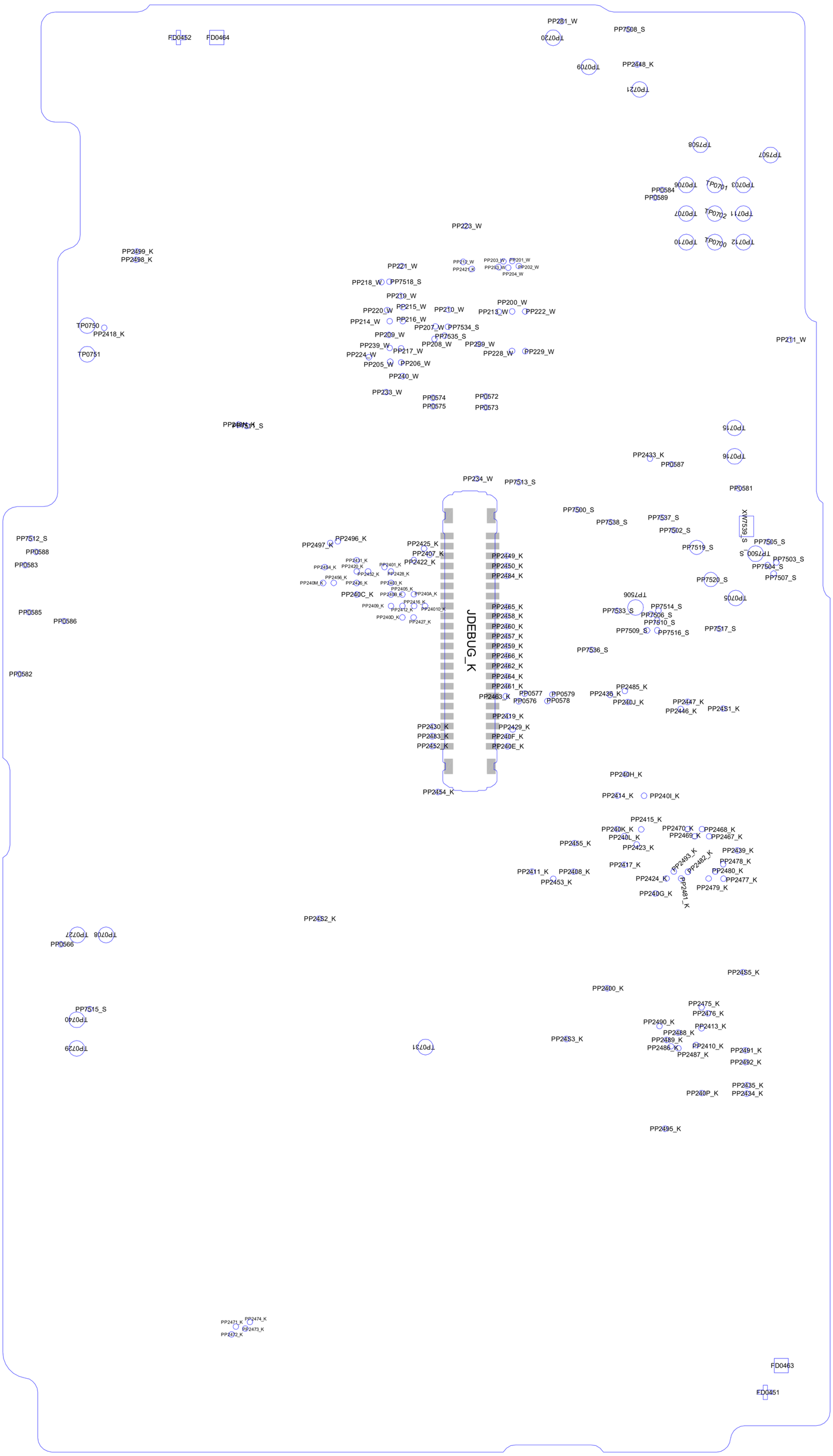

U1000
U_ROSE_R
U4700
U6300
U3700
U2700
U1400
PA_HB_K
PA_UHB_K
GPLR_L_K
U_5G_L_W
U_5G_U_W
FLANT5_K
FLANT6_K
FLBPF8_R
FLHPF6_R
J_INT_BOT
SH0002
PP0642
FD0412
FD0413
FD0410
FD0415
FD0406

J7010
JLAT
J7600
J7700
J7800
J7830
J7400
J8100
J7200
J7900
J7300
J8000
J8200
JUAT
U2600
U4500
U3920
U4100
U4120
U4410
Y1000
SB0301
SB0302
SB0303
SB0304
SB0305
no_reflies+1
no_reflies+2
no_reflies+3


PA_LB_K
XCVR_K
MIMODS_K
BB_K
NFC_S
U_WLAN_W
J_SIM_K
ETIC_K
U5000
BBPMU_K
DSM_HB_K
DSM_LB_K
GPLR_U_K
L_LNA_K
FLANT2_K
FLANT4_K
EEPROM_K
VIN1_K
no_refdes+3
no_refdes+2
no_refdes+1
J_INT_TOP


FD0452
FD0464
PP281_W
TP0720
PP7508_S
TP0709
PP2448_K
TP0721
TP7508
TP7507
TP0706
TP0703
TP0701
PP0584
PP0589
TP0707
TP0702
TP0711
TP0710
TP0700
TP0712
PP223_W
PP2499_K
PP2498_K
PP221_W
PP212_W
PP2421_K
PP203_W
PP201_W
PP203_K
PP202_W
PP204_W
PP218_W
PP7518_S
PP219_W
PP200_W
PP215_W
PP220_W
PP210_W
PP213_W
PP222_W
PP214_W
PP216_W
PP207_W
PP7534_S
TP0750
PP2418_K
PP209_W
PP7535_S
PP211_W
PP239_W
PP208_W
PP299_W
TP0751
PP224_W
PP217_W
PP228_W
PP229_W
PP205_W
PP206_W
PP240_W
PP233_W
PP0574
PP0572
PP0575
PP0573
TP0715
PP2433_K
TP0716
PP0587
PP234_W
PP7513_S
PP0581
PP7500_S
PP7538_S
PP7537_S
XW7536_S
PP7502_S
PP7512_S
PP2496_K
PP2497_K
PP2425_K
PP7519_S
PP7505_S
PP0588
PP2407_K
PP2422_K
PP2449_K
TP7500_S
PP7503_S
PP0583
PP2450_K
PP7504_S
PP2484_K
PP7520_S
PP7507_S
PP240C_K
TP7506
TP0705
PP0585
PP7533_S
PP7514_S
PP7506_S
PP0586
PP7510_S
PP7509_S
PP7516_S
PP7517_S
PP2465_K
PP2458_K
PP7536_S
PP0582
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PP2461_K
PP2485_K
PP2463_K
PP0577
PP0579
PP2436_K
PP0576
PP0578
PP240J_K
PP2447_K
PP2446_K
PP2451_K
PP2419_K
PP2430_K
PP2429_K
PP2483_K
PP240F_K
PP2452_K
PP240E_K
PP240H_K
PP2454_K
PP2414_K
PP240I_K
PP2415_K
PP240K_K
PP2470_K
PP2468_K
PP240L_K
PP2469_K
PP2467_K
PP2455_K
PP2423_K
PP2439_K
PP2403_K
PP2482_K
PP2478_K
PP2417_K
PP2411_K
PP2408_K
PP2480_K
PP2424_K
PP2477_K
PP2453_K
PP2481_K
PP2479_K
PP240G_K
PP2452_K
TP0727
TP0708
PP0566
PP2455_K
PP2400_K
PP7515_S
TP0740
PP2475_K
PP2476_K
PP2490_K
PP2413_K
PP2488_K
TP0729
TP0731
PP2453_K
PP2489_K
PP2410_K
PP2486_K
PP2491_K
PP2487_K
PP2492_K
PP2435_K
PP240P_K
PP2434_K
PP2495_K
PP2471_K
PP2474_K
PP2473_K
PP2472_K
FD0463
FD0451

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

D42/D43 MLB_TOP_AVUS: CRB

LAST_MODIFICATION=Fri May 3 22:17:26 2019

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6	9	BOOTSTRAPPING	MLB_TOP	08/01/2018
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8	11	SOC: PCIE	MLB_TOP	08/06/2018
9	12	SOC: ISP	mlb_top	10/02/2018
10	13	SOC: Display	mlb_top	10/02/2018
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18	26	NAND	mlb_top	10/02/2018
19	27	SYSTEM POWER: PMU Bucks (1/4)	MLB_TOP	08/01/2018
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23	31	SYSTEM POWER: Boost	mlb_top	10/02/2018
24	37	CAMERA: PMU1 (1/2)	mlb_top	10/02/2018
25	38	CAMERA: PMU1 (2/2)	mlb_top	10/02/2018
26	39	CAMERA: DISCRETE (DIGITAL)	mlb_top	10/02/2018
27	41	CAMERA: DISCRETE (ANALOG)	mlb_top	10/02/2018
28	44	PEARL: Power	rigel	10/03/2018
29	45	SENSORS: Top	mlb_top	10/02/2018
30	47	AUDIO: CODEC (1/2)	mlb_top	10/02/2018
31	48	AUDIO: CODEC (2/2)	mlb_top	10/02/2018
32	55	CG POWER: Touch	mlb_top	10/02/2018
33	59	I/O: VDDM Comparators	mlb_top	10/02/2018
34	61	I/O: Gecko	mlb_top	10/02/2018
35	62	I/O: USB PD	mlb_top	10/02/2018
36	63	I/O: Hydra	mlb_top	10/02/2018
37	65	Interposer: Top	mlb_top	10/02/2018
38	66	Interposer: Aliases	mlb_top	09/05/2018
39	69	B2B: Battery (North)	mlb_top	10/02/2018
40	72	B2B: Camera Wide (ON)	mlb_top	10/02/2018
41	73	B2B: Camera Tele [MT]	mlb_top	10/02/2018
42	74	B2B: Camera SWide (MB)	mlb_top	10/02/2018
43	76	B2B: Camera Fcam	mlb_top	10/02/2018
44	77	B2B: Strobe + Side Button	mlb_top	10/02/2018
45	78	B2B: Pearl Romeo + Juliet	mlb_top	10/02/2018
46	79	B2B: Pearl Rosaline + Sensor	mlb_top	10/02/2018
47	80	B2B: CG Display	mlb_top	09/07/2018
48	81	B2B: CG Touch	mlb_top	10/02/2018
49	82	B2B: Dock	mlb_top	10/02/2018
50	100	ALIASES: Power (Top)	MLB_TOP	08/02/2018
51	110	ALIASES: FF ISP	mlb_top	10/02/2018
52	111	ALIASES: FF GPIO	MLB_TOP	08/02/2018
53	120	ALIASES: I2C - AP	mlb_top	10/02/2018
54	121	ALIASES: I2C - AOP/SMC	MLB_TOP	08/06/2018
55	130	ALIASES: I2C - Camera	mlb_top	10/02/2018
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58	200	Radios	MLB_TOP	07/19/2018
59	1	SCH,RADIO_MLB_ICE_LOFT		
60	2	HB SPAD		05/01/2018
61	3	UHB MLB SPAD		05/01/2018
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63	5	LOWER ANTENNA FEEDS		05/01/2018
64	6	ANTENNA SYSTEM		05/01/2018
65	1	FRONT PAGE		
66	2	MODULE		
67	3	FILTERS MATCHING		
68	1	FEM MODULES		
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MCO: 056-08495

BOM: 639-07383 (ULTIMATE,ROW,D42)
BOM: 639-07386 (ULTIMATE,NA+CH,D42)
BOM: 639-07384 (EXTREME,ROW,D42)
BOM: 639-07387 (EXTREME.NA+CH,D42)
BOM: 639-07385 (MAX,ROW,D42)
BOM: 639-07388 (MAX,NA+CH,D42)

BOM: 639-06878 (ULTIMATE,ROW,D43)
BOM: 639-06907 (ULTIMATE,NA+CH,D43)
BOM: 639-06879 (EXTREME,ROW,D43)
BOM: 639-06908 (EXTREME.NA+CH,D43)
BOM: 639-06880 (MAX,ROW,D43)
BOM: 639-06909 (MAX,NA+CH,D43)

EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR (MLB_TOP,639-06878,ULTIMATE,ROW,D42)	LNCH	CRITICAL	ULTIMATE_ROW_D42
825-7691	1	EEEE FOR (MLB_TOP,639-06907,ULTIMATE,US+CH,D42)	LNDJ	CRITICAL	ULTIMATE_USCH_D42
825-7691	1	EEEE FOR (MLB_TOP,639-06879,EXTREME,ROW,D42)	LNCR	CRITICAL	EXTREME_ROW_D42
825-7691	1	EEEE FOR (MLB_TOP,639-06908,EXTREME,US+CH,D42)	LNDX	CRITICAL	EXTREME_USCH_D42
825-7691	1	EEEE FOR (MLB_TOP,639-06880,MAX,ROW,D42)	LND4	CRITICAL	MAX_ROW_D42
825-7691	1	EEEE FOR (MLB_TOP,639-06909,MAX,US+CH,D42)	LNF8	CRITICAL	MAX_USCH_D42
825-7691	1	EEEE FOR (MLB_TOP,639-06878,ULTIMATE,ROW,D43)	L1W2	CRITICAL	ULTIMATE_ROW_D43
825-7691	1	EEEE FOR (MLB_TOP,639-06907,ULTIMATE,US+CH,D43)	L38J	CRITICAL	ULTIMATE_USCH_D43
825-7691	1	EEEE FOR (MLB_TOP,639-06879,EXTREME,ROW,D43)	L1WF	CRITICAL	EXTREME_ROW_D43
825-7691	1	EEEE FOR (MLB_TOP,639-06908,EXTREME,US+CH,D43)	L38W	CRITICAL	EXTREME_USCH_D43
825-7691	1	EEEE FOR (MLB_TOP,639-06880,MAX,ROW,D43)	L1WR	CRITICAL	MAX_ROW_D43
825-7691	1	EEEE FOR (MLB_TOP,639-06909,MAX,US+CH,D43)	L397	CRITICAL	MAX_USCH_D43

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-04448	1	SCH,MLB_TOP,D43	SCH	CRITICAL	?
820-01682	1	PCB,MLB_TOP,D43	PCB	CRITICAL	?

Sub Designs

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D43	RADIO_MLB_ICE_LOFT	0.83.0	S	2019_04_30_16:40:16
D42	ROSE_MLB	0.56.0	S	2019_05_02_11:27:27
D42	LAA_MLB	0.28.0	S	2019_04_26_11:43:12

NAND

Ultimate

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00360	1	TOSHIBA, 3Dv4,256Gb, Ultimate	U2600	CRITICAL	ULTIMATE

Extreme

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00342	1	HYNIX, 3Dv4,512Gb, Extreme	U2600	CRITICAL	EXTREME

Max

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00343	1	HYNIX, 3Dv4, 512Gb, Max	U2600	CRITICAL	MAX

Global Capacitors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00148	138S00149	ALT_PARTS	ALL	0402-3T,10.5uF@1V, Kyocera
138S00150	138S00149	ALT_PARTS	ALL	0402-3T,10.5uF@1V, SEMCO
138S00151	138S00149	ALT_PARTS	ALL	0402-3T,10.5uF@1V, TY

CRITICAL PART#	COMMENT
138S00149	0402-3T,10.5uF@1V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00138	138S00139	ALT_PARTS	ALL	0201,3uF@1V, Kyocera
138S00164	138S00139	ALT_PARTS	ALL	0201,3uF@1V, TY
138S00280	138S00139	ALT_PARTS	ALL	0201,3uF@1V,SAM

CRITICAL PART#	COMMENT
138S00139	0201,3uF@1V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00221	138S00146	ALT_PARTS	ALL	0402,5.1uF@3V, Kyocera

CRITICAL PART#	COMMENT
138S00146	0402,5.1uF@3V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00003	138S00048	ALT_PARTS	ALL	0402,15uF,6.3V, MURATA

CRITICAL PART#	COMMENT
138S00048	0402,15uF,6.3

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00140	138S00141	ALT_PARTS	ALL	0201,1.1uF@3V, Kyocera
138S00268	138S00141	ALT_PARTS	ALL	0201,1.1uF@3V, SEMCO

CRITICAL PART#	COMMENT
138S00141	0201,1.1uF@3V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	ALT_PARTS	ALL	CAP,CER,X5R,4UF,20%,6.3V,0201,H=0.55,TY
138S00117	138S00071	ALT_PARTS	ALL	CAP,CER,X5R,4UF,20%,6.3V,0201,H=0.55,KYO

CRITICAL PART#	COMMENT
138S00071	CAP,CER,X5R,4UF,20%,6.3V,0201,H=0.55

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00128	138S00133	ALT_PARTS	ALL	01005,0.47uF,6.3V,Murata
138S00269	138S00133	ALT_PARTS	ALL	01005,0.47uF,6.3V,Taiyo

CRITICAL PART#	COMMENT
138S00133	01005,0.47uF, 6.3V

20uF/26uF Dual Source

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S00279	7	CAP,20UF,4V,0402,SEMCO	C1708,C1709,C1733,C1736,C1970,C2711,C2712	CRITICAL	CAP_20UF_SAMCO_ALT
138S00279	7	CAP,20UF,4V,0402,SEMCO	C2721,C2722,C2751,C2752,C3700,C3701,C3925	CRITICAL	CAP_20UF_SAMCO_ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00144	138S00279	CAP_20UF_SAMCO_ALT	C1708,C1709,C1733,C1736,C1970,C2711,C2712	0402,20uF,4V,SEMCO
138S00144	138S00279	CAP_20UF_SAMCO_ALT	C2721,C2722,C2751,C2752,C3700,C3701,C3925	0402,20uF,4V,SEMCO

15uF Single Source

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S00003	9	CAP,15UF,6.3V,0402,MURATA	C1734,C1735,C2723,C2724,C2753,C3801,C3811,C3813,C3735	CRITICAL	CAP_15UF_SINGLE_SOURCE
138S00003	8	CAP,15UF,6.3V,0402,MURATA	C1763,C1765,C1766,C3835,C3836,C3837,C3837,C3923	CRITICAL	CAP_15UF_SINGLE_SOURCE

Global Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S00070	377S00001	ALT_PARTS	ALL	TVS,BIDIR,5.8V,6PF,01005
377S00140	377S00001	ALT_PARTS	ALL	TVS,BIDIR,5V,6PF,01005,SEMTECH
377S00061	377S0183	ALT_PARTS	ALL	TVS,BIDIR,5.8V,0201
377S00080	377S0183	ALT_PARTS	ALL	TVS,BIDIR,5V,5PF,0201,SEMTECH
377S00173	377S0183	ALT_PARTS	ALL	TVS,BIDIR,5V,6.5PF,0201,SEMTECH
377S0168	377S00129	ALT_PARTS	ALL	SUPPRESS,TRANS,6.8V,100PF,AMETECH,01005
155S00400	155S00200	ALT_PARTS	ALL	FERR BD,150OHM,25%,200MA,0.70HM DCR,01005
155S00194	155S00200	ALT_PARTS	ALL	FERR BD,150OHM,25%,200MA,0.650HM DCR,01005
155S0755	155S00341	ALT_PARTS	ALL	FERR BD,240OHM,25%,200MA,1ohm DCR,01005
155S00437	155S00402	ALT_PARTS	ALL	FERR BD,330OHM,25%,1.5A,55MOHM DCR,0201
152S00366	152S00402	ALT_PARTS	ALL	IND,PWR,1.0UH,20%,1.8A,160MOHM,TAIYO,1608
131S00329	131S00025	ALT_PARTS	ALL	CAP,C0G,1000PF,2%,25V,TAIYO,0201
132S00185	132S0316	ALT_PARTS	ALL	CAP,CER,X5R,0.1UF,20%,6.3V,01005
132S00232	132S00014	ALT_PARTS	ALL	CAP,X5R,0.22UF,10%,6.3V,TAIYO,01005
132S00233	132S00014	ALT_PARTS	ALL	CAP,X5R,0.22UF,10%,6.3V,TAIYO,01005
132S00088	132S0639	ALT_PARTS	ALL	CAP,X5R,0.47uF,20%,25V,0201,TAIYO
138S0739	138S0706	ALT_PARTS	ALL	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S0945	138S0706	ALT_PARTS	ALL	CAP,CER,X5R,1UF,20%,10V,0201,KYOCERA
138S00264	138S00008	ALT_PARTS	ALL	CAP,X5R,1.5UF,20%,6.3V.TAIYO,0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00284	138S00136	ALT_PARTS	ALL	CAP,X5R,2.2UF,20%,10V.KYO,0201
138S00049	138S0831	ALT_PARTS	ALL	CAP,CER,X5R,2.2UF,20%,6.3V,0201
138S00138	138S00164	ALT_PARTS	ALL	CAP,X5R,4UF,20%,4V.KYO,0201
138S00139	138S00164	ALT_PARTS	ALL	CAP,X5R,4UF,20%,4V.MURATA,0201

CRITICAL PART#	COMMENT
377S00001	TVS,BIDIR,5.8V,6PF,01005
377S0183	TVS,BIDIR,5.8V,0201
377S00129	SUPRESS,TRANS,6.8V,100PF,01005
155S00200	FERR BD,150OHM,25%,200MA,0.70HM DCR,01005
155S00402	FERR BD,33OHM,25%,1.5A,55MOHM DCR,0201
152S00402	IND,PWR,1.0UH,20%,1.8A,160MOHM,1608
118S00144	RES,MF,24KOHM,1%,200PPM,1/32W,01005
131S00025	CAP,C0G,1000PF,2%,25V,0201
132S0316	CAP,X5R,0.1UF,20%,6.3V,01005
132S00014	CAP,X5R,0.22UF,10%,6.3V,01005
132S0639	CAP,CER,X5R,0.47UF,20%,25V,0201
138S0706	CAP,X5R,1UF,20%,10V,0201
138S00264	CAP,X5R,1.5UF,20%,6.3V,0201
138S00008	CAP,X5R,1.5UF,20%,6.3V,0201
138S0831	CAP,CER,X5R,2.2UF,20%,6.3V,0201
138S00284	CAP,CER,X5R,2.2UF,20%,10V,0201
138S00164	CAP,X5R,4UF,20%,4V,0201

AVUS INDUCTORS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00721	152S00876	ALT_PARTS	ALL	Taiyo,IND,M1D,1UH,3.6A,60MΩ,2016
152S00930	152S00897	ALT_PARTS	ALL	Cyntec,IND,CPL3,0.1UH,6.1A,27MΩ,2016
152S00826	152S00821	ALT_PARTS	ALL	Taiyo,IND,M1D,1UH,2.2A,60MΩ,2012
152S00831	152S00818	ALT_PARTS	ALL	Taiyo,IND,M1D,0.22UH,5.3A,40MΩ,1608
152S00994	152S00987	ALT_PARTS	ALL	Taiyo,IND,M1D,1UH,1.5A,67MΩ,2012
152S00991	152S00984	ALT_PARTS	ALL	Taiyo,IND,M1D,0.47UH,3.5A,34MΩ,1614
152S00992	152S00985	ALT_PARTS	ALL	Taiyo,IND,M1D,0.47UH,4.6A,45MΩ,2012
152S00989	152S00982	ALT_PARTS	ALL	Taiyo,IND,M6LT,0.47UH,2.8A,70MΩ,1608

CRITICAL PART#	COMMENT
152S00876	Cyntec,IND
152S00897	Taiyo,IND
152S00821	Cyntec,IND
152S00818	Cyntec,IND
152S00987	Cyntec,IND
152S00984	Cyntec.IND
152S00985	Cyntec,IND
152S00982	Cyntec,IND

Display CMC's

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00415	155S00524	ALT_PARTS	ALL	CMC,35O_OHM,7GHZ,TDK

CRITICAL PART#	COMMENT
155S00524	FLT,NOISE,35O_OHM,7GHZ,50MA,0403,MURATA

Multi-Vendor Criticals

CRITICAL PART#	COMMENT
197S0446	XTAL,24MHZ,30PPM,9.5PF,60 OHM MAX,1612
155S00168	FLTR,NOISE,65 OHMZ,3.4OHM,0.7-2GHZ,0605
377S0106	SUPPR,TRANS,VARISTOR,12V,33PF,01005
155S0576	FERR BD,10 OHM,50%,750MA,0.07 DCR,01005
155S00341	FERR BD,240 OHM,25%,200MA,0.9 DCR,01005
107S0257	THERMISTOR,NTC,10K OHM,1%,B=3435,01005
118S0608	RES,MF,1KOHM,1/32W,1%,01005
118S00064	RES,MF,11KOHM,1/32W,1%,01005
118S00022	RES,MF,41.2KOHM,1%,1/32W,01005
118S0637	RES,MF,82OHM,1%,1/32W,01005
118S00068	RES,MF,1.3 MOHM,1%,200PPM,1/20W,0201
117S0055	RES,MF,2MOHM,1/20W,5%,0201,SMD

CRITICAL PART#	COMMENT
131S00353	CAP,CER,NPO/C0G,10PF,5%,16V,01005
131S0220	CAP,CER,NPO/C0G,12PF,5%,16V,01005
131S00293	CAP,CER,NPO/C0G,12PF,5%,16V,01005
131S0225	CAP,CER,NPO/C0G,15PF,5%,16V,01005
131S00290	CAP,CER,NPO/C0G,15PF,5%,16V,01005
131S00378	CAP,CER,NPO/C0G,22PF,5%,16V,01005
131S0223	CAP,CER,NPO/C0G,27PF,5%,16V,01005
131S0804	CAP,CER,NPO/C0G.27PF,5%,25V,0201
131S00291	CAP,CER,NPO/C0G,27PF,5%,16V,01005
131S00023	CAP,CER,NPO/C0G,39PF,5%,25V,01005
131S0216	CAP,CER,NPO/C0G,47PF,5%,16V,01005
131S00323	CAP,CER,NPO/COG,56PF,5%,25V,01005
131S0643	CAP,CER,NPO/C0G,56PF,5%,25V,01005
131S0635	CAP,CER,NPO/C0G,68PF,5%,16V,01005
131S00303	CAP,CER,NPO/COG,100PF,5%,16V,01005
131S0307	CAP,CER,NPO/C0G,100PF,5%,16V,01005
131S00053	CAP,CER,NPO/C0G,220PF,5%,10V,01005
132S0249	CAP,CER,X7R,220PF,10%,10V,01005
131S00170	CAP,CER,NPO/C0G,220PF,5%,25V,01005
131S0883	CAP,CER,NPO/C0G,220PF,2%,50V,0201
132S00258	CAP,CER,X7R,330PF,10%,16V,01005
132S0275	CAP,CER,X5R,470PF,10%,10V,01005
132S0318	CAP,CER,X5R,820PF,10%,10V,01005
132S0296	CAP,CER,X5R,1000PF,10%,6.3V,01005
132S0396	CAP,CER,X5R,1000PF,10%,10V,01005

CRITICAL PART#	COMMENT
132S0245	CAP,CER,X5R,0.01UF,10%,6.3V,01005
132S00093	CAP,CER,X5R,0.022UF,20%,6.3V,01005
132S00025	CAP,CER,X5R,0.047UF,20%,6.3V,01005
132S0664	CAP,CER,0.047UF,10%,25V,X5R,0201
132S0316	CAP,CER,X5R,0.1UF,20%,6.3V,01005
132S00185	CAP,CER,X5R,0.1UF,20%,6.3V,01005
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0534	CAP,CER,X5R,0.1UF,10%,25V,0201
132S00008	CAP,CER,X7R,0.1UF,10%,50V,0402
132S0304	CAP,CER,X5R,0.22UF,20%,6.3V,0201
138S00014	CAP,CER,1UF,20%,16V,X5R,0201,H=0.39MM
138S0692	CAP,CER,X5R,1UF,20%,6.3V,0201
138S0683	CAP,CER,X5R,1UF,10%,25V,0402
138S00070	CAP,X5R,4.7UF,20%,25V,0402
138S0652	CAP,CER,X5R,4.7UF,20%,6.3V,H=0.65MM,0402
138S0979	CAP,CER,X5R,10UF,20%,10V,0402,H=0.65MM

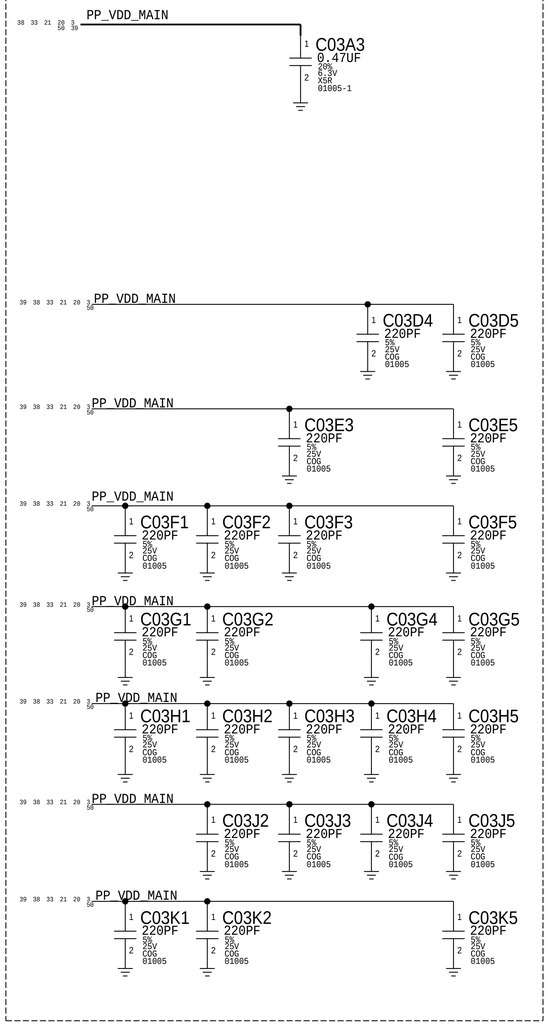
XTAL Alternate

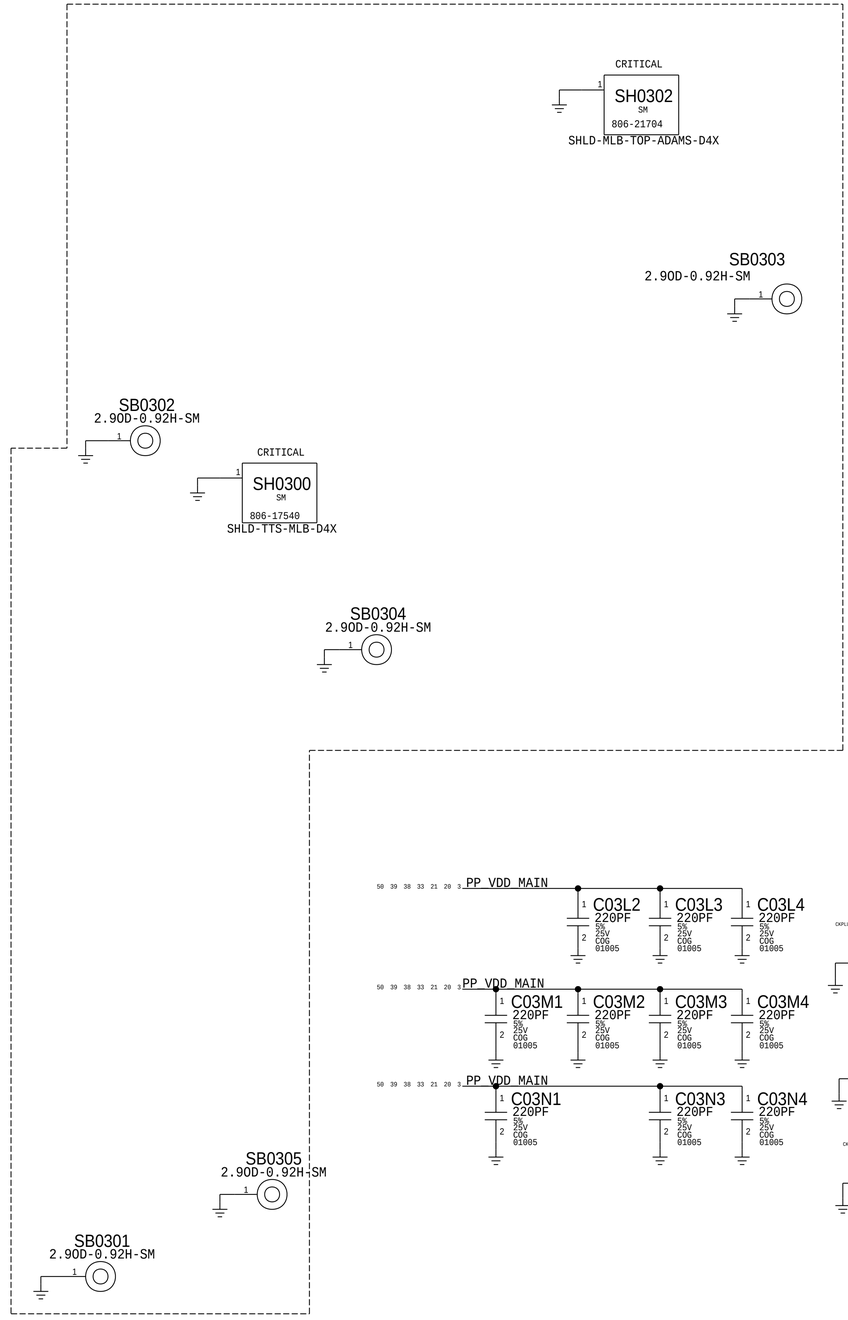
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0612	197S00118	ALT_PARTS	Y1000	XTAL, 24M, 1612
197S00120	197S00118	ALT_PARTS	Y1000	XTAL, 24M, 1612

Cebu

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00592	339S00591	ALT_PARTS	U1000	CEBU,4GB,16NM,M
339S00593	339S00591	ALT_PARTS	U1000	CEBU,4GB,16NM,H
339S00594	339S00591	ALT_PARTS	U1000	CEBU,4GB,16NM,S

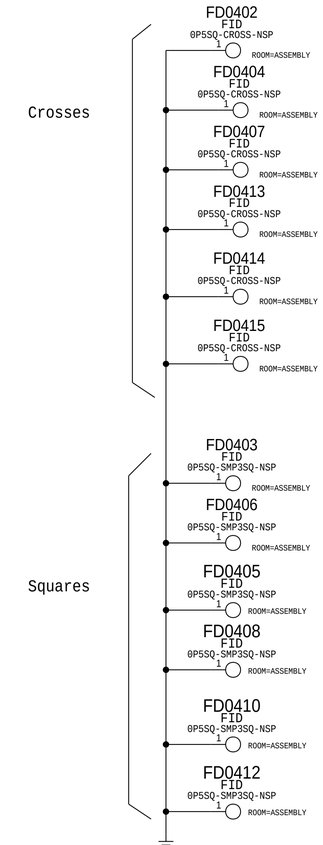
AC Return Steering - 50x

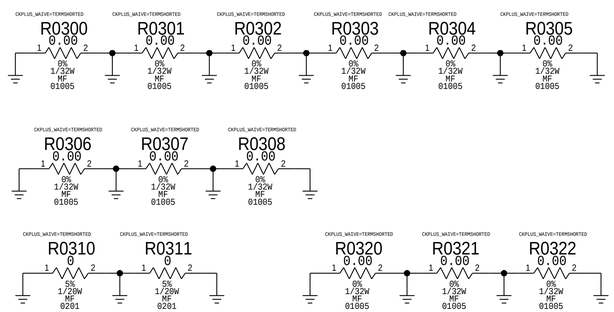




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-03604	25	SPACER,INTERPOSER,SMALL,X891	MP0400-MP0424	CRITICAL	COMMON

FIDUCIALS





RADIOS

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_{N}X Calculates dielectric distance from stackup, standard distance is used unless 1.5 defined	EXAMPLE: 1,3,5,7L,8L 10L 1.5,2,3
A_DIELECTRIC_{N}XD XV,XVL,_X Calculates dielectric distance from Hybrid Table and stackup, standard distance is used unless 1. defined	EXAMPLE: 2,12L,30-50,7V,8VL-10VL 2,2D,4D,4V
A_DIELECTRIC_{N}XN_{N}XOUT Calculates dielectric distance from stackup, standard distance is used unless 1. is defined	EXAMPLE: 2_4,3L_5L ?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
90_OHM	P	A_90_OHM_DIFF	DP:DP_*90*	?
GENERIC_DP	P	GENERIC_DP	DP:DP_MIC*,DP_PENROSE*,DP_NTC_*,DP_MTR_RREF*	?
GENERIC_DP	P	GENERIC_DP	DP:DP_ANALOG*SENSE*	?
NC_GENERIC_DP	P	GENERIC_DP	DP:DP_NC*	?
PWR_DP	P	PWR_DP	DP:DP_CODEC_AOUT*	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GND	S	MSAP_YIELD	GND	?
LPDP_WIDE	S	A_DIELECTRIC_3X	DP:DP_*90_LPDP*_WIDE*	?
LPDP_SWIDE	S	A_DIELECTRIC_3X	DP:DP_*90_LPDP*_SWIDE*	?
LPDP_TELE	S	A_DIELECTRIC_3X	DP:DP_*90_LPDP*_TELE*	?
LPDP_FCAM	S	A_DIELECTRIC_3X	DP:DP_*90_LPDP*_FCAM*	?
MIPI_DISPLAY	S	A_DIELECTRIC_3X	DP:DP_*90_MIPI*DISPLAY*	?
MIPI_IRCAM	S	A_DIELECTRIC_3X	DP:DP_*90_MIPI*_IRCAM*	?
PCIE_NAND	S	A_DIELECTRIC_3X	DP:DP_*90_PCIE*_NAND*	?
PCIE_WLAN	S	A_DIELECTRIC_3X	DP:DP_*90_PCIE*_WLAN*	?
PCIE_BB	S	A_DIELECTRIC_3X	DP:DP_*90_PCIE*_BB*	?
HYDRA_DP	S	A_DIELECTRIC_3X	DP:DP_*90_*HYDRA*	?
MIKEYBUS_DP	S	A_DIELECTRIC_3X	DP:DP_*90_*MIKEYBUS*	?
USB_DP	S	A_DIELECTRIC_3X	DP:DP_*90_*USB*	?
CLK	S	A_DIELECTRIC_1.5X	CLK_AP*,CLK_BBPMU*,CLK_CAM*,CLK_GPIO*,CLK_ISP*,CLK_PMU_TO*	?
CLK_PMU_XTAL	S	A_DIELECTRIC_1.5X	CLK_PMU_XTAL*	?
CLK_SPMI	S	A_DIELECTRIC_1.5X	SPMI*CLK*	?
ANALOG_FB	S	A_DIELECTRIC_1.5X	ANALOG_FB*	?
SWITCHING	S	A_DIELECTRIC_1.5X	LX*_BUCK*	?
MIC1_DP	S	A_DIELECTRIC_1.5X	DP:DP_*MIC1*	?
MIC2_DP	S	A_DIELECTRIC_1.5X	DP:DP_*MIC2*	?
MIC3_DP	S	A_DIELECTRIC_1.5X	DP:DP_*MIC3*	?
MIC4_DP	S	A_DIELECTRIC_1.5X	DP:DP_*MIC4*	?
MIC1	S	DEFAULT	PP_*MIC1*,*MIC1*FILT_RET*	?
MIC2	S	DEFAULT	PP_*MIC2*,*MIC2*FILT_RET*	?
MIC3	S	DEFAULT	PP_*MIC3*,*MIC3*FILT_RET*	?
MIC4	S	DEFAULT	PP_*MIC4*,*MIC4*FILT_RET*	?
PENROSE_DP	S	A_DIELECTRIC_1.5X	DP:DP_*PENROSE*	?
VSS_PMU_RTC	S	DEFAULT	VSS_PMU_RTC	?

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
SWITCHING	GND	DEFAULT
S_PWR_200UM	GND	DEFAULT
S_PWR_SHAPE	GND	DEFAULT
S_PWR_100UM	S_PWR_100UM	100UM-249UM_SPACING
S_PWR_200UM	S_PWR_200UM	100UM-249UM_SPACING
S_PWR_SHAPE	S_PWR_SHAPE	250UM+_SPACING
LPDP_WIDE	LPDP_WIDE	A_DIELECTRIC_2X
LPDP_SWIDE	LPDP_SWIDE	A_DIELECTRIC_2X
LPDP_TELE	LPDP_TELE	A_DIELECTRIC_2X
LPDP_FCAM	LPDP_FCAM	A_DIELECTRIC_2X
MIPI_DISPLAY	MIPI_DISPLAY	A_DIELECTRIC_2X
MIPI_IRCAM	MIPI_IRCAM	A_DIELECTRIC_2X
PCIE_NAND	PCIE_NAND	A_DIELECTRIC_2X
PCIE_WLAN	PCIE_WLAN	A_DIELECTRIC_2X
PCIE_BB	PCIE_BB	A_DIELECTRIC_2X
HYDRA_DP	HYDRA_DP	A_DIELECTRIC_2X
USB_DP	USB_DP	A_DIELECTRIC_2X
MIC1_DP	MIC1	DEFAULT
MIC2_DP	MIC2	DEFAULT
MIC3_DP	MIC3	DEFAULT
MIC4_DP	MIC4	DEFAULT
PENROSE_DP	PENROSE_DP	DEFAULT
CLK_PMU_XTAL	VSS_PMU_RTC	DEFAULT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
E_LPDP_WIDE	E	DIFF_PAIR	DP:DP_*90_LPDP*_WIDE*	?
E_LPDP_SWIDE	E	DIFF_PAIR	DP:DP_*90_LPDP*_SWIDE*	?
E_LPDP_TELE	E	DIFF_PAIR	DP:DP_*90_LPDP*_TELE*	?
E_LPDP_FCAM	E	DIFF_PAIR	DP:DP_*90_LPDP*_FCAM*	?
E_MIPI_DISPLAY	E	DIFF_PAIR	DP:DP_*90_MIPI*DISPLAY*	?
E_MIPI_IRCAM	E	DIFF_PAIR	DP:DP_*90_MIPI*_IRCAM*	?
E_PCIE_NAND	E	DIFF_PAIR	DP:DP_*90_PCIE*_NAND*	?
E_PCIE_WLAN	E	DIFF_PAIR	DP:DP_*90_PCIE*_WLAN*	?
E_PCIE_BB	E	DIFF_PAIR	DP:DP_*90_PCIE*_BB*	?
E_USB_DP	E	DIFF_PAIR	DP:DP_*90_*USB*,DP_90*HYDRA*	?
E_MIKEY_DP	E	DIFF_PAIR	DP:DP_*90_*MIKEY*	?
E_PWR_DP	E	GENERIC_DP	DP:DP_CODEC_AOUT*	?
E_GENERIC	E	GENERIC_DP	DP:DP_MIC*,DP_PENROSE*,DP_NTC_*,DP_*MTR*,DP_ANALOG*SENSE*	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DEFAULT_THICK	P	DEFAULT_THICK	*MIC*BIAS*	?

SYSTEM WIDE

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_DEFAULT	P	PWR_DEFAULT	PP_CPU_PCORE_LVCC,PP_GPU_LVCC	?
PWR_80UM	P	PWR_80UM	PP1V8_ALWAYS,PP3V3_USB_DEBUG*,PP3V3_USB	?
PWR_100UM	P	PWR_100UM	PP1V2_S2	?
PWR_200UM	P	PWR_200UM	PP1V8_S2,PP3V0_S2,PP1V8_IO	?
PWR_300UM	P	PWR_300UM	PP1V8_NFC_S2	?
PWR_SHAPE	P	PWR_SHAPE	LX*_BUCK*	?
PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAIN,PP_VDD_BOOST	?
PWR_SHAPE	P	PWR_SHAPE	PP1V1_S2	?
PWR_SHAPE	P	PWR_SHAPE	PP1V2_S4	?
S_PWR_100UM	S	100UM-249UM_SPACING	PP1V2_S2	?
S_PWR_200UM	S	100UM-249UM_SPACING	PP1V8_S2,PP3V0_S2,PP1V8_IO	?
S_PWR_300UM	S	250UM+_SPACING	PP1V8_NFC_S2	?
S_PWR_SHAPE	S	250UM+_SPACING	PP_VDD_MAIN,PP_VDD_BOOST	?
S_PWR_SHAPE	S	250UM+_SPACING	PP1V1_S2	?
S_PWR_SHAPE	S	250UM+_SPACING	PP1V2_S4	?

SOC

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_80UM	P	PWR_80UM	PP0V8_SOC_FIXED_PCIE_REFBUF,PP0V8_USB_DEBUG,PP_VDD_LOW_USB_DEBUG	?
PWR_80UM	P	PWR_80UM	PP1V2_SOC_PCIE_REFBUF,PP1V8_XTAL	?
PWR_100UM	P	PWR_100UM	PP_VDDIO12_GRP5	?
PWR_200UM	P	PWR_200UM	PP1V2_SOC,PP0V6_VDDQL_S1,PP1V8_FMON_R,PP1V8_ULPPLL_R	?
PWR_SHAPE	P	PWR_SHAPE	PP_CPU_ECORE,PP_CPU_PCORE,PP_DCS_S1	?
PWR_SHAPE	P	PWR_SHAPE	PP_GPU,PP_SOC_S1,PP0V8_SOC_FIXED_S1	?
PWR_SHAPE	P	PWR_SHAPE	PP0V7_VDD_LOW_FLPPLL_R,PP0V7_VDD_LOW_S2	?
PWR_SHAPE	P	PWR_SHAPE	PP0V7_VDD_LOW_ULPPLL_R,PP_AVE_S1,PP_DISP_S1,PP_SRAM_S1	?
S_PWR_100UM	S	100UM-249UM_SPACING	PP_VDDIO12_GRP5	?
S_PWR_200UM	S	100UM-249UM_SPACING	PP1V2_SOC,PP0V6_VDDQL_S1,PP1V8_FMON_R,PP1V8_ULPPLL_R	?
S_PWR_SHAPE	S	250UM+_SPACING	PP_CPU_ECORE,PP_CPU_PCORE,PP_DCS_S1	?
S_PWR_SHAPE	S	250UM+_SPACING	PP_GPU,PP_SOC_S1,PP0V8_SOC_FIXED_S1	?
S_PWR_SHAPE	S	250UM+_SPACING	PP0V7_VDD_LOW_FLPPLL_R,PP0V7_VDD_LOW_S2	?
S_PWR_SHAPE	S	250UM+_SPACING	PP0V7_VDD_LOW_ULPPLL_R,PP_AVE_S1,PP_DISP_S1,PP_SRAM_S1	?

NAND

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_80UM	P	PWR_80UM	PP1V8_IO_NAND_*	?
PWR_100UM	P	PWR_100UM	ANALOG_NAND_ZQ*,ANALOG_PCIE_NAND_RESREF	?
PWR_SHAPE	P	PWR_SHAPE	PP0V9_NAND*,PP2V63_NAND,PP1V2_IO_NAND,PP_VDDIO_2_NAND_R	?
S_PWR_100UM	S	100UM-249UM_SPACING	ANALOG_NAND_ZQ*,ANALOG_PCIE_NAND_RESREF	?
S_PWR_SHAPE	S	250UM+_SPACING	PP0V9_NAND*,PP2V63_NAND,PP1V2_IO_NAND,PP_VDDIO_2_NAND_R	?

PMU

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_SHAPE	P	PWR_SHAPE	PP0V9_S1	?
S_PWR_SHAPE	S	250UM+_SPACING	PP0V9_S1	?

RADIO_MLB_ICE_LOFT

DOMAIN (E,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_L10_SE	50_LAA_TO_ANT_LAT
P	A_50_THIN_L10_SE	50_ANT5_LAA

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_ANT1_CPLR_IN	Y
50_THIN_L10	S	A_DIELECTRIC_2X_50_THIN_L10_SE	50_ANT5_LAA,50_LAA_TO_ANT_LAT	Y

LAA_MLB

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF S,P,E	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN_L10	S	A_DIELECTRIC_2X_50_THIN_L10_SE	50_LAA_TO_ANT_LAT,50_WLAN_A*	?

DOMAIN (E,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_LAA_TO_XCVR*
P	A_50_THIN_L10_SE	50_LAA_TO_ANT_LAT,50_WLAN_A_*

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.062
ISL6	ISL5,ISL7	50	0.038
ISL8	ISL7,ISL9	50	0.029
BOTTOM	ISL9	50	0.062

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
TOP	ISL3	50	0.174
ISL3	TOP,ISL5	50	0.091
ISL5	ISL3,ISL7	50	0.104
ISL7	ISL5,ISL9	50	0.098
ISL8	ISL7,ISL9	50	0.029
BOTTOM	ISL8	50	0.174

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_WIDE_L1_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.062
ISL5	ISL3,ISL7	50	0.104
ISL6	ISL5,ISL7	50	0.038
ISL7	ISL5,ISL9	50	0.098
ISL8	ISL7,ISL9	50	0.029
BOTTOM	ISL9	50	0.062

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_THIN_L10		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.062
ISL5	ISL3,ISL7	50	0.104
ISL6	ISL5,ISL7	50	0.038
ISL8	ISL7,ISL9	50	0.029

ISL5_WIDE ->

CAPPED RULE EXAMPLE:SMD2ALL,SMD_TO_SMD;MVIA2ALL,SHAPE2ALL	LAYER EX:ALL,EXT,INT,TOP,BOT	VALUE (MM)	RULE NAME(S) EXAMPLE: 2D,2V,3DL-5DL,3VL
LINE2SMD	?	0.070	2,2D,4D,4V
MVIA2MVIA	?	=0.065	2D,4D,4V
MVIA2SMD	?	=0.070	2,2D,4D,4V
MVIA2SHAPE	?	=0.070	2,2D,4D,4V
SMD2SMD	?	0.070	2,2D,4D,4V
SMD2SHAPE	?	0.070	2,2D,4D,4V
LINE2LINE	ALL	0.290	4V
LINE2MVIA	EXT	0.150	4V
LINE2MVIA	INT	0.279	4V
LINE2LINE	TOP	0.160	2
LINE2MVIA	EXT	0.075	2
LINE2MVIA	INT	0.120	2
MVIA2MVIA	EXT	0.080	2
MVIA2MVIA	INT	0.060	2

Probe Points - TOP

METROLOGY

Removed: PAD_MTR_ANALOG_TEST_P

Removed: PAD_MTR_ANALOG_TEST_N

LVCC

PP_GPU_LVCC: ProbePoint removed, Access through MLB_BOT

50 19 PP_GPU — XW0510 SHORT-10L-0.05MM-SM (1, 2) — PP_GPU_LVCC 38

PP_CPU_Pcore: ProbePoint removed,Access through MLB_BOT

50 19 PP_CPU_PCORE — XW0511 SHORT-10L-0.05MM-SM (1, 2) — PP_CPU_PCORE_LVCC 38

BUMP SENSE

17	ANALOG_GPU_SENSEN	PP0653	P2MM-NSM SM 1 PP ROOM=TEST
14	ANALOG_GPU_SENSEP	PP0613	P2MM-NSM SM 1 PP ROOM=TEST
17	ANALOG_CPU_PCORE_SENSEN	PP0651	P2MM-NSM SM 1 PP ROOM=TEST
14	ANALOG_CPU_PCORE_SENSEP	PP0612	P2MM-NSM SM 1 PP ROOM=TEST
17	ANALOG_SOC_SENSE_N	PP0616	P2MM-NSM SM 1 PP ROOM=TEST
14	ANALOG_SOC_SENSE_P	PP0614	P2MM-NSM SM 1 PP ROOM=TEST
16	ANALOG_DCS_SENSEP	PP0617	P2MM-NSM SM 1 PP ROOM=TEST
17	ANALOG_VDDQL_DCS_SENSEN	PP0652	P2MM-NSM SM 1 PP ROOM=TEST
16	ANALOG_VDDQL_SENSEP	PP0618	P2MM-NSM SM 1 PP ROOM=TEST

SOC Debug

22 7	CLK_AP_TO_PMU_TST_CLKOUT	PP0600	P2MM-NSM SM 1 PP ROOM=TEST
7 6	GPIO_BOARD_ID0	PP0601	P2MM-NSM SM 1 PP ROOM=TEST
47 9	GPIO_ISP_TO_DISPLAY_FLASH_INT	PP0602	P2MM-NSM SM 1 PP ROOM=TEST

Removed: PROBE_SOC_DEBUG3. Repurposed GPIO

Removed PP0604: PROBE_DFU_STATUS.: Add for Proto1

22 7	IO_PMU_TO_AP_PRE_UVLO_L	PP0605	P2MM-NSM SM 1 PP ROOM=TEST

PMU

13	PROBE_AOP_TO_DDR_SLEEP1	PP0620	P2MM-NSM SM 1 PP ROOM=TEST
36 22 7	IO_PMU_TO_AP_HYDRA_ACTIVE_READY	PP0622	P2MM-NSM SM 1 PP ROOM=TEST
22 13	IO_AP_TO_PMU_RESET	PP0623	P2MM-NSM SM 1 PP ROOM=TEST
22 7	IO_AP_TO_PMU_SOCHOT_L	PP0624	P2MM-NSM SM 1 PP ROOM=TEST
56 13	SWD_NUB_BI_PMU_SWDIO	PP0691	P2MM-NSM SM 1 PP ROOM=TEST

NAND

18 7	SWD_AP_BI_NAND_SWDIO	PP0660	P2MM-NSM SM 1 PP ROOM=TEST
18 11 6	SPI0_AP_FROM_S4E_MISO_BOOT_CONFIG2	PP0662	P2MM-NSM SM 1 PP ROOM=TEST
18 7	IO_AP_TO_NAND_RESET_L	PP0665	P2MM-NSM SM 1 PP ROOM=TEST

PCIE

18 8	90_PCIE0_AP_TO_NAND_REFCLK_P	PP0630	P2MM-NSM SM 1 PP ROOM=TEST
18 8	90_PCIE0_AP_TO_NAND_REFCLK_N	PP0631	P2MM-NSM SM 1 PP ROOM=TEST

Sensors

56 29	GPIO_AOP_FROM_IMU_DATARDY	PP0644	P2MM-NSM SM 1 PP ROOM=TEST

Rigel

28	PP_RIGEL_BUCK_BOOST_A	PP0680	P2MM-NSM SM 1 PP ROOM=TEST
28	PP_RIGEL_BUCK_BOOST_B	PP0681	P2MM-NSM SM 1 PP ROOM=TEST

CCG SWD

56 35	GPIO_AP_TO_CCG2_SWCLK	PP0640	P2MM-NSM SM 1 PP ROOM=TEST

ADAMS

25 9	SPMI_ISP_TO_CAM_PMU1_CLK	PP0645	P2MM-NSM SM 1 PP ROOM=TEST
25 9	SPMI_ISP_BI_CAM_PMU1_DATA	PP0646	P2MM-NSM SM 1 PP ROOM=TEST
27 26 25	GPIO_CAM_PMU1_TO_SWIDE_LDO_EN	PP0642	P2MM-NSM SM 1 PP ROOM=TEST
27 26 25	GPIO_CAM_PMU1_TO_WIDE_LDO_EN	PP0643	P2MM-NSM SM 1 PP ROOM=TEST
27 26 25	GPIO_CAM_PMU1_TO_FCAM_LDO_EN	PP0647	P2MM-NSM SM 1 PP ROOM=TEST
27 25	GPIO_CAM_PMU1_TO_TELE_LDO_EN	PP0648	P2MM-NSM SM 1 PP ROOM=TEST

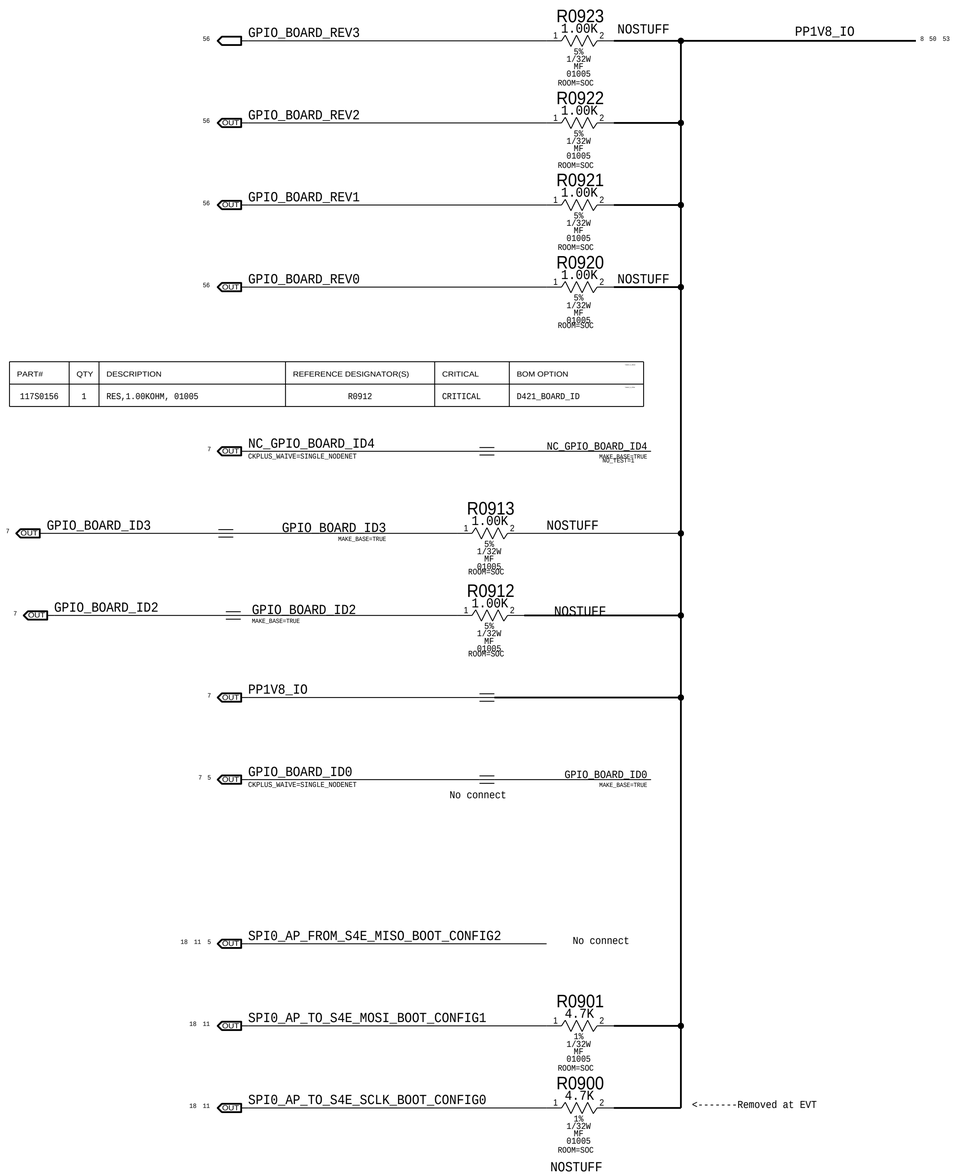
VALIDATION PP's

34 13	GPIO_NUB_FROM_GECKO_IRQ_L	PP0690	P2MM-NSM SM 1 PP ROOM=TEST
35 13	GPIO_NUB_FROM_CCG2_INT_L	PP0667	P2MM-NSM SM 1 PP ROOM=TEST
22 13	CLK_PMU_TO_AOP_32K	PP0694	P2MM-NSM SM 1 PP ROOM=TEST
36 11	UART7_AP_FROM_ACCESSORY_RXD	PP0696	P2MM-NSM SM 1 PP ROOM=TEST
31 11	SPI3_AP_FROM_CODEC_MISO	PP0697	P2MM-NSM SM 1 PP ROOM=TEST
31 11	SPI3_AP_TO_CODEC_MOSI	PP0698	P2MM-NSM SM 1 PP ROOM=TEST
31 11	SPI3_AP_TO_CODEC_CS_L	PP0699	P2MM-NSM SM 1 PP ROOM=TEST
56 31	GPIO_AOP_TO_CODEC_CLP_EN	PP0670	P2MM-NSM SM 1 PP ROOM=TEST
56 31	GPIO_AOP_TO_CODEC_RESET_L	PP0671	P2MM-NSM SM 1 PP ROOM=TEST
56 31	GPIO_AP_FROM_CODEC_INT_L	PP0672	P2MM-NSM SM 1 PP ROOM=TEST
36 11	UART7_AP_TO_ACCESSORY_TXD	PP0673	P2MM-NSM SM 1 PP ROOM=TEST
28 25	GPIO_CAM_PMU1_TO_RIGEL_ENABLE	PP0674	P2MM-NSM SM 1 PP ROOM=TEST
28 25 22	GPIO_CAM_PMU1_FROM_RIGEL_INT	PP0675	P2MM-NSM SM 1 PP ROOM=TEST

علي البحر-فريق المهارد حلب تلي

TOP BOARD ONLY CONFIGURATION IS D42/D43 MLB
BOTTOM BOARD SELECTS ICE/MAV

BOOTSTRAPPING:BOARD REV
BOARD ID
BOOT CONFIG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0156	1	RES,1.00KOHM, 01005	R0912	CRITICAL	D421_BOARD_ID

SELECTED -->

Board Rev[3:0] Float=Low I PU=High	3	2	1	0
PreProto	1	1	1	1
Proto 1	1	1	1	0
(Spare)	1	1	0	1
Proto 2	1	1	0	0
(Spare)	1	0	1	1
EVT	1	0	1	0
(Spare)	0	1	1	1
Carrier	0	1	1	0
(Spare)	0	0	1	1
DVT	0	0	1	0
(Spare)	0	0	0	1
PVT	0	0	0	0

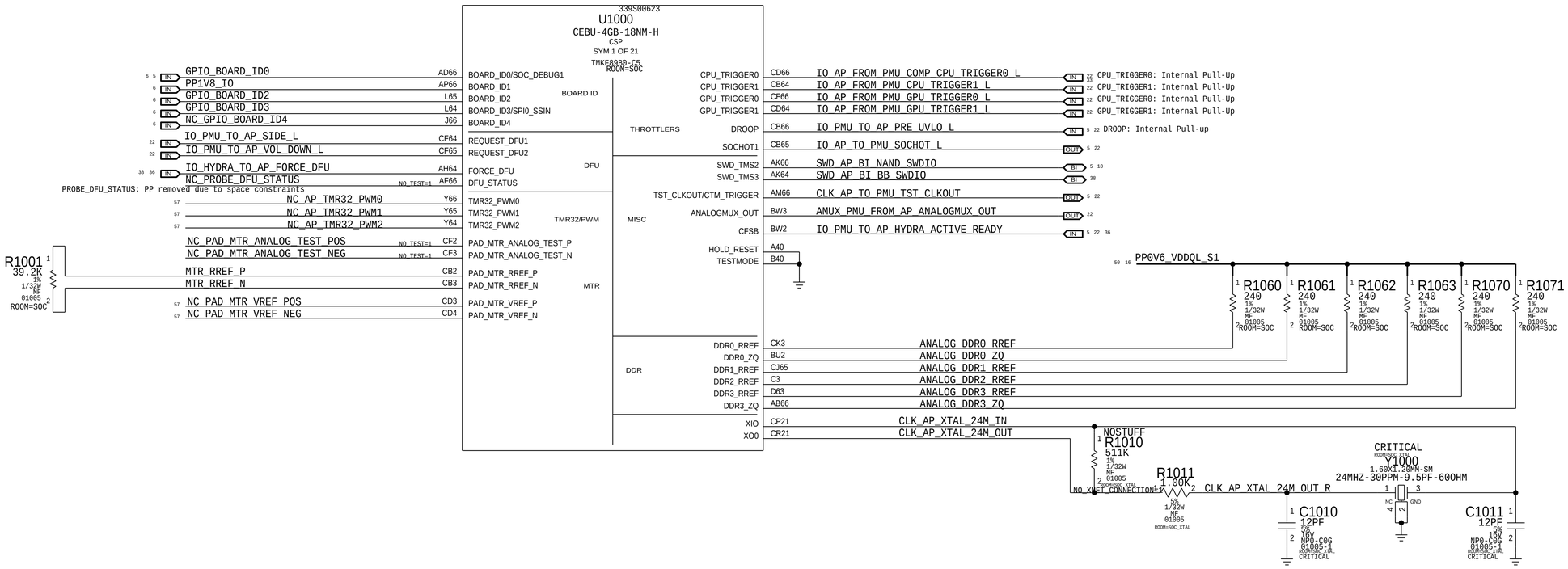
DEFAULT -->

		Board ID[4:0] Float=Low I PU=High				
		4	3	2	1	0
	BoardID[4:0]	**Unused**	**0** = ICE, **1** = MAV	**00** = None **01** = x1367/9 **11** = x1364/8 **10** = x1403		**0** = MLB, **1** = DEV
MLB N104	**5'b00100**	0	0	1	0	0
DEV N104	**5'b00101**	0	0	1	0	1
MLB D42	**5'b01110**	0	1	1	1	0
DEV D42	**5'b01111**	0	1	1	1	1
MLB D421	**5'b00110**	0	0	1	1	0
DEV D421	**5'b00111**	0	0	1	1	1
MLB D43	**5'b01010**	0	1	0	1	0
DEV D43	**5'b01011**	0	1	0	1	1
MLB D431	**5'b00010**	0	0	0	1	0
DEV D431	**5'b00011**	0	0	0	1	1

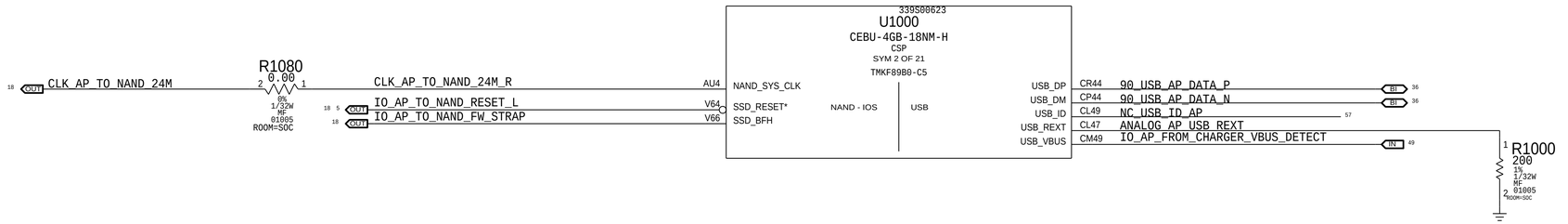
POR -->
Proto Builds -->

				Boot Config[2:0] Float=Low I PU=High		
	Usage	**MHz**	**Test**	**2**	**1**	**0**
SPI0 NOR	--	12		0	0	0
SPI0 NOR	--	12	Test	0	0	1
SPI0 NAND	POR	12		0	1	0
SPI0 NAND	Proto	12	Test	0	1	1
SPI0 NOR	--	40		1	0	0
SPI0 NOR	--	40	Test	1	0	1
SPI0 NOR	--	6		1	1	0
SPI0 NOR	--	6	Test	1	1	1

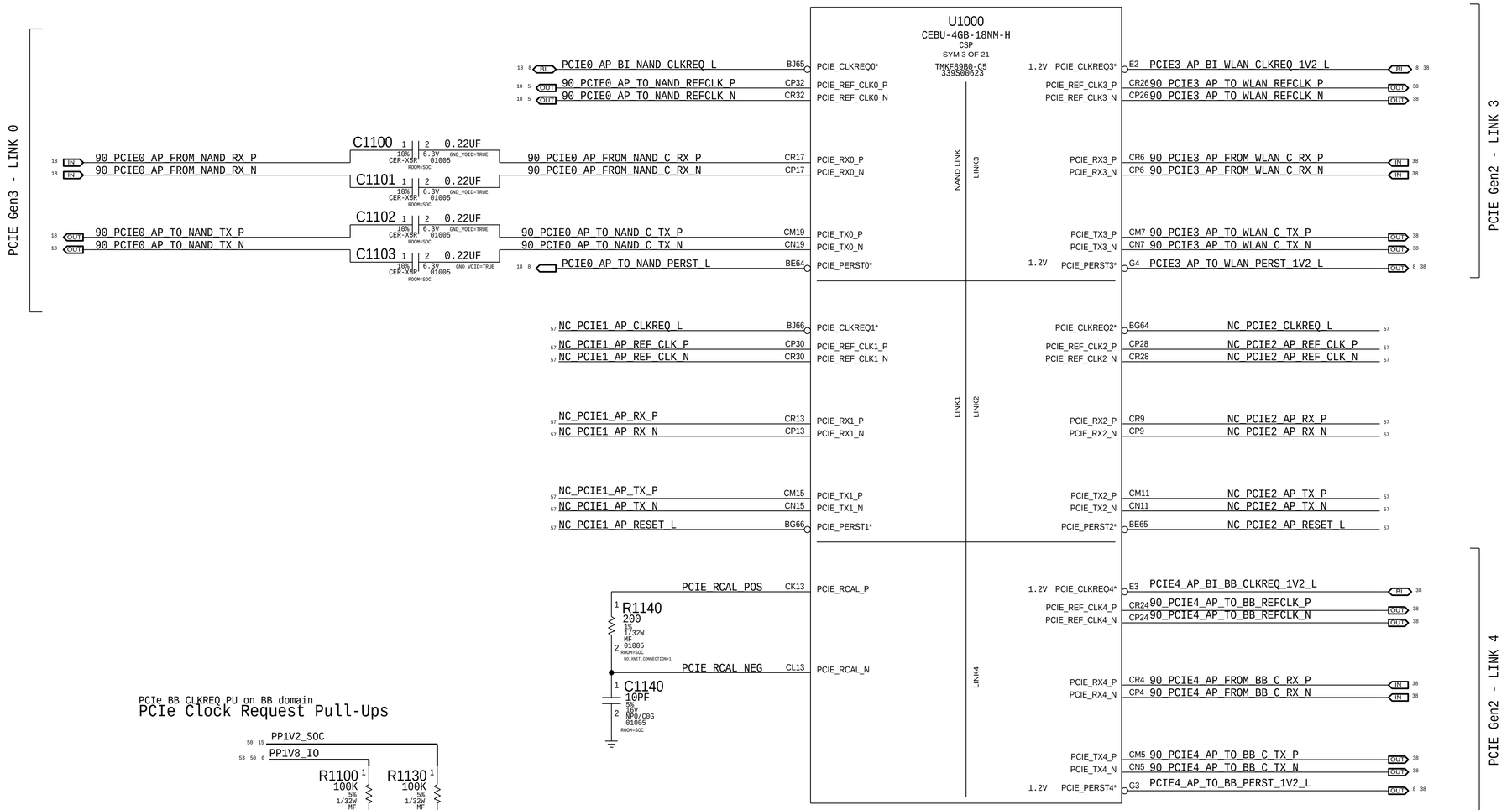
SOC: Misc



SOC: NAND + USB

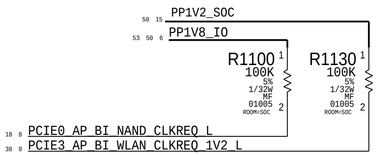


SOC: PCIe

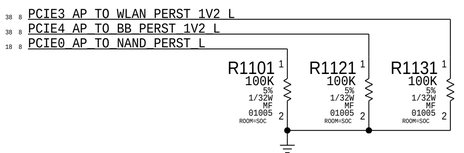


PCIe BB CLKREQ PU on BB domain

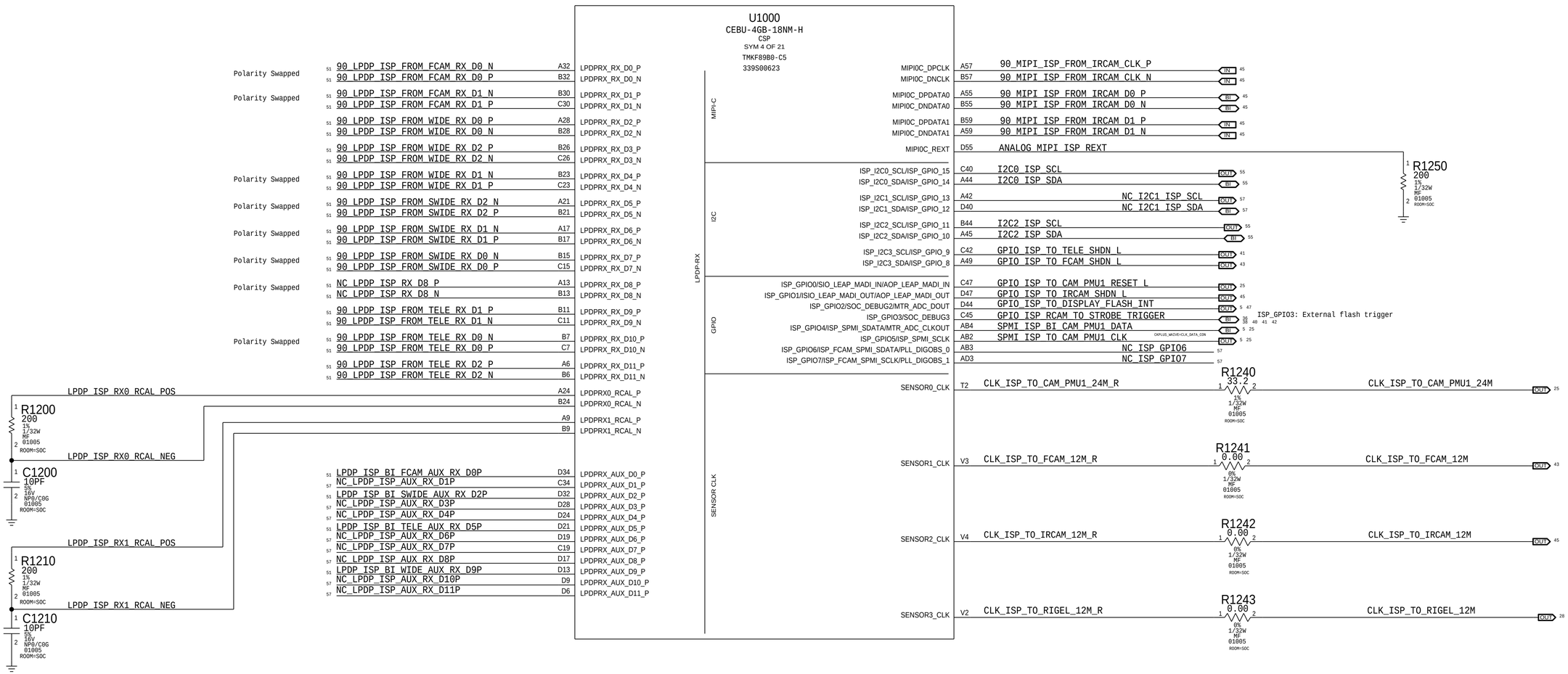
PCIe Clock Request Pull-Ups



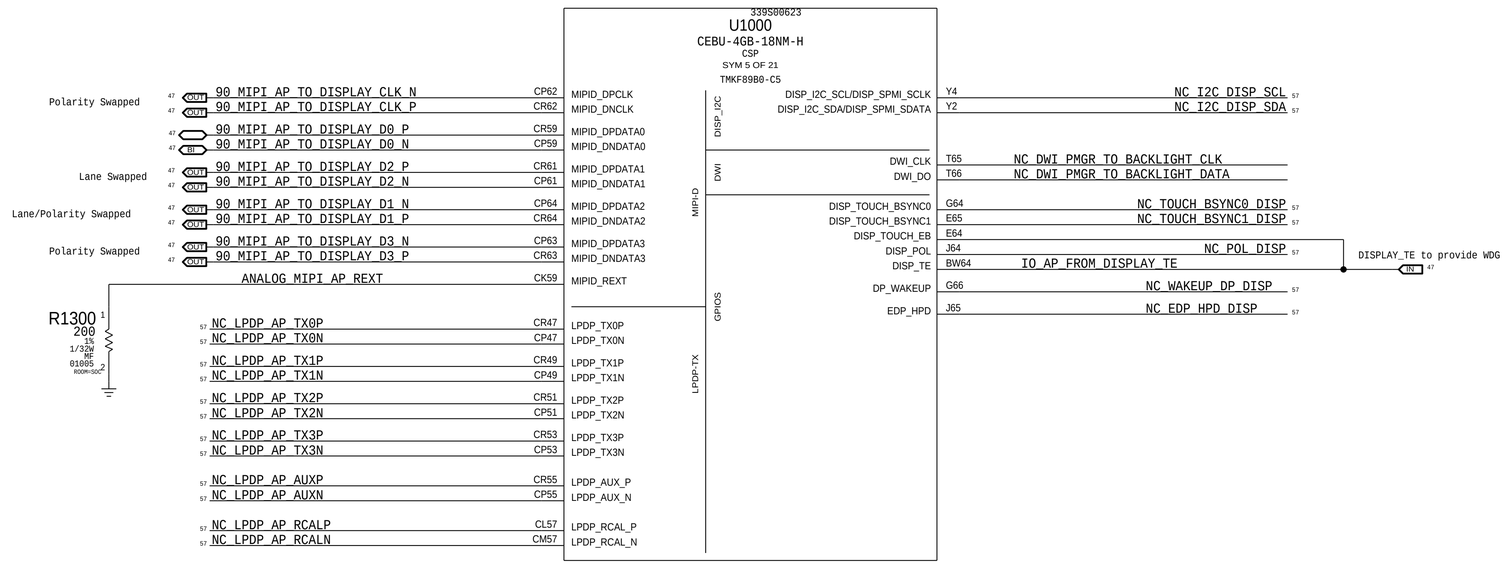
PCIe Reset Pull-Downs



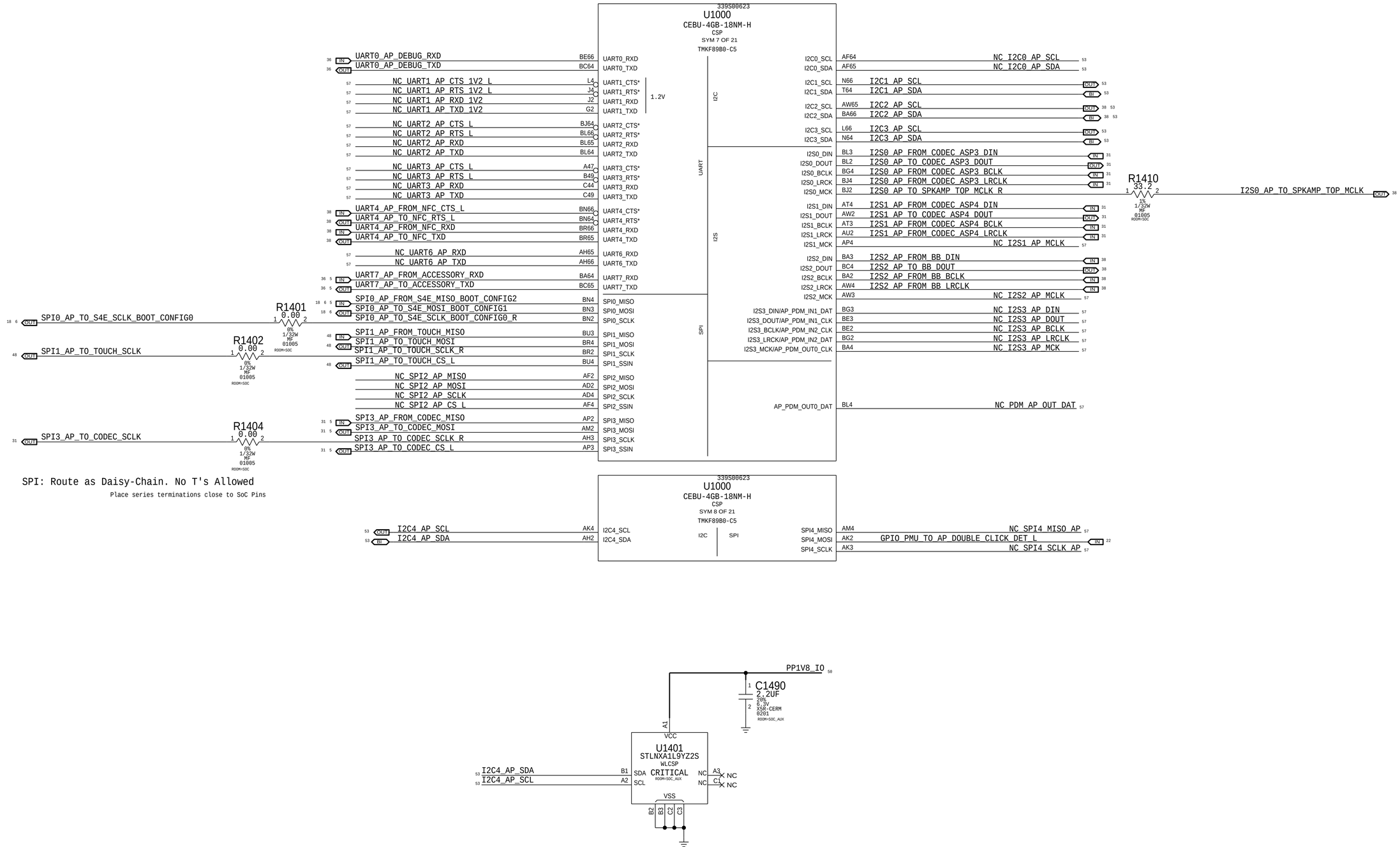
SOC: ISP


U1000
CEBU-4GB-18NM-H
CSP
SYM 4 OF 21
TMKF89B0-C5
339S00623
LPDPRX
MIPI-C
I2C
GPIO
SENSOR CLK
90_LPDP_ISP_FROM_FCAM_RX_D0_N A32 LPDPRX_RX_D0_P
90_LPDP_ISP_FROM_FCAM_RX_D0_P B32 LPDPRX_RX_D0_N
90_LPDP_ISP_FROM_FCAM_RX_D1_N B30 LPDPRX_RX_D1_P
90_LPDP_ISP_FROM_FCAM_RX_D1_P C30 LPDPRX_RX_D1_N
90_LPDP_ISP_FROM_WIDE_RX_D0_P A28 LPDPRX_RX_D2_P
90_LPDP_ISP_FROM_WIDE_RX_D0_N B28 LPDPRX_RX_D2_N
90_LPDP_ISP_FROM_WIDE_RX_D2_P B26 LPDPRX_RX_D3_P
90_LPDP_ISP_FROM_WIDE_RX_D2_N C26 LPDPRX_RX_D3_N
90_LPDP_ISP_FROM_WIDE_RX_D1_N B23 LPDPRX_RX_D4_P
90_LPDP_ISP_FROM_WIDE_RX_D1_P C23 LPDPRX_RX_D4_N
90_LPDP_ISP_FROM_SWIDE_RX_D2_N A21 LPDPRX_RX_D5_P
90_LPDP_ISP_FROM_SWIDE_RX_D2_P B21 LPDPRX_RX_D5_N
90_LPDP_ISP_FROM_SWIDE_RX_D1_N A17 LPDPRX_RX_D6_P
90_LPDP_ISP_FROM_SWIDE_RX_D1_P B17 LPDPRX_RX_D6_N
90_LPDP_ISP_FROM_SWIDE_RX_D0_N B15 LPDPRX_RX_D7_P
90_LPDP_ISP_FROM_SWIDE_RX_D0_P C15 LPDPRX_RX_D7_N
NC_LPDP_ISP_RX_D8_P A13 LPDPRX_RX_D8_P
NC_LPDP_ISP_RX_D8_N B13 LPDPRX_RX_D8_N
90_LPDP_ISP_FROM_TELE_RX_D1_P B11 LPDPRX_RX_D9_P
90_LPDP_ISP_FROM_TELE_RX_D1_N C11 LPDPRX_RX_D9_N
90_LPDP_ISP_FROM_TELE_RX_D0_N B7 LPDPRX_RX_D10_P
90_LPDP_ISP_FROM_TELE_RX_D0_P C7 LPDPRX_RX_D10_N
90_LPDP_ISP_FROM_TELE_RX_D2_P A6 LPDPRX_RX_D11_P
90_LPDP_ISP_FROM_TELE_RX_D2_N B6 LPDPRX_RX_D11_N
Polarity Swapped
LPDP_ISP_RX0_RCAL_POS A24 LPDPRX0_RCAL_P
B24 LPDPRX0_RCAL_N
A9 LPDPRX1_RCAL_P
B9 LPDPRX1_RCAL_N
LPDP_ISP_RX0_RCAL_NEG
LPDP_ISP_RX1_RCAL_POS
LPDP_ISP_RX1_RCAL_NEG
R1200 200 1% 1/32W MF 01005 ROOM=SOC
C1200 10PF 5% 10V NP0/C0G 01005 ROOM=SOC
R1210 200 1% 1/32W MF 01005 ROOM=SOC
C1210 10PF 5% 10V NP0/C0G 01005 ROOM=SOC
LPDP_ISP_BI_FCAM_AUX_RX_D0P D34 LPDPRX_AUX_D0_P
NC_LPDP_ISP_AUX_RX_D1P C34 LPDPRX_AUX_D1_P
LPDP_ISP_BI_SWIDE_AUX_RX_D2P D32 LPDPRX_AUX_D2_P
NC_LPDP_ISP_AUX_RX_D3P D28 LPDPRX_AUX_D3_P
NC_LPDP_ISP_AUX_RX_D4P D24 LPDPRX_AUX_D4_P
LPDP_ISP_BI_TELE_AUX_RX_D5P D21 LPDPRX_AUX_D5_P
NC_LPDP_ISP_AUX_RX_D6P D19 LPDPRX_AUX_D6_P
NC_LPDP_ISP_AUX_RX_D7P C19 LPDPRX_AUX_D7_P
NC_LPDP_ISP_AUX_RX_D8P D17 LPDPRX_AUX_D8_P
LPDP_ISP_BI_WIDE_AUX_RX_D9P D13 LPDPRX_AUX_D9_P
NC_LPDP_ISP_AUX_RX_D10P D9 LPDPRX_AUX_D10_P
NC_LPDP_ISP_AUX_RX_D11P D6 LPDPRX_AUX_D11_P
MIPI0C_DPCLK A57 90_MIPI_ISP_FROM_IRCAM_CLK_P
MIPI0C_DNCLK B57 90_MIPI_ISP_FROM_IRCAM_CLK_N
MIPI0C_DPDATA0 A55 90_MIPI_ISP_FROM_IRCAM_D0_P
MIPI0C_DNDATA0 B55 90_MIPI_ISP_FROM_IRCAM_D0_N
MIPI0C_DPDATA1 B59 90_MIPI_ISP_FROM_IRCAM_D1_P
MIPI0C_DNDATA1 A59 90_MIPI_ISP_FROM_IRCAM_D1_N
MIPI0C_REXT D55 ANALOG_MIPI_ISP_REXT
R1250 200 1% 1/32W MF 01005 ROOM=SOC
ISP_I2C0_SCL/ISP_GPIO_15 C40 I2C0_ISP_SCL
ISP_I2C0_SDA/ISP_GPIO_14 A44 I2C0_ISP_SDA
ISP_I2C1_SCL/ISP_GPIO_13 A42 NC_I2C1_ISP_SCL
ISP_I2C1_SDA/ISP_GPIO_12 D40 NC_I2C1_ISP_SDA
ISP_I2C2_SCL/ISP_GPIO_11 B44 I2C2_ISP_SCL
ISP_I2C2_SDA/ISP_GPIO_10 A45 I2C2_ISP_SDA
ISP_I2C3_SCL/ISP_GPIO_9 C42 GPIO_ISP_TO_TELE_SHDN_L
ISP_I2C3_SDA/ISP_GPIO_8 A49 GPIO_ISP_TO_FCAM_SHDN_L
ISP_GPIO0/SIO_LEAP_MADI_IN/AOP_LEAP_MADI_IN C47 GPIO_ISP_TO_CAM_PMU1_RESET_L
ISP_GPIO1/ISIO_LEAP_MADI_OUT/AOP_LEAP_MADI_OUT D47 GPIO_ISP_TO_IRCAM_SHDN_L
ISP_GPIO2/SOC_DEBUG2/MTR_ADC_DOUT D44 GPIO_ISP_TO_DISPLAY_FLASH_INT
ISP_GPIO3/SOC_DEBUG3 C45 GPIO_ISP_RCAM_TO_STROBE_TRIGGER
ISP_GPIO4/ISP_SPMI_SDATA/MTR_ADC_CLKOUT AB4 SPMI_ISP_BI_CAM_PMU1_DATA
ISP_GPIO5/ISP_SPMI_SCLK AB2 SPMI_ISP_TO_CAM_PMU1_CLK
ISP_GPIO6/ISP_FCAM_SPMI_SDATA/PLL_DIGOBS_0 AB3 NC_ISP_GPIO6
ISP_GPIO7/ISP_FCAM_SPMI_SCLK/PLL_DIGOBS_1 AD3 NC_ISP_GPIO7
ISP_GPIO3: External flash trigger
SENSOR0_CLK T2 CLK_ISP_TO_CAM_PMU1_24M_R
R1240 33.2 1% 1/32W MF 01005 ROOM=SOC
CLK_ISP_TO_CAM_PMU1_24M
SENSOR1_CLK V3 CLK_ISP_TO_FCAM_12M_R
R1241 0.00 0% 1/32W MF 01005 ROOM=SOC
CLK_ISP_TO_FCAM_12M
SENSOR2_CLK V4 CLK_ISP_TO_IRCAM_12M_R
R1242 0.00 0% 1/32W MF 01005 ROOM=SOC
CLK_ISP_TO_IRCAM_12M
SENSOR3_CLK V2 CLK_ISP_TO_RIGEL_12M_R
R1243 0.00 0% 1/32W MF 01005 ROOM=SOC
CLK_ISP_TO_RIGEL_12M

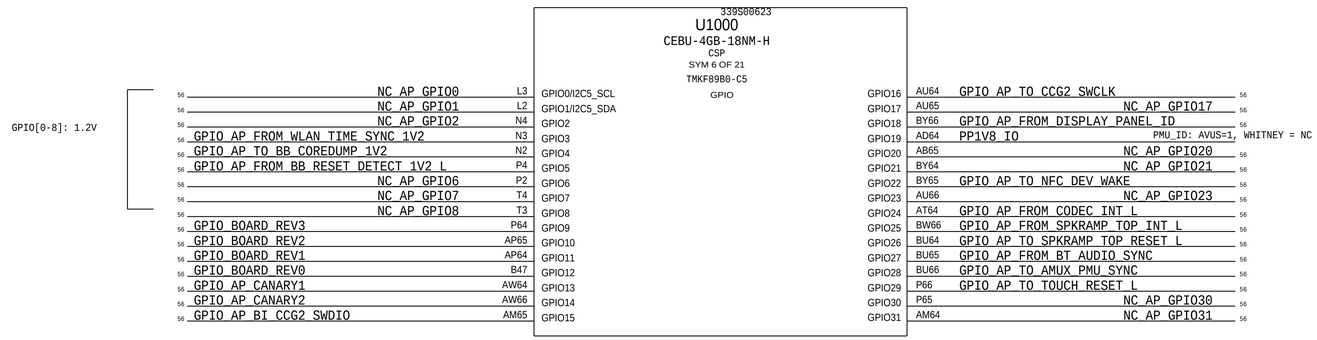
SOC: Display


339S00623
U1000
CEBU-4GB-18NM-H
CSP
SYM 5 OF 21
TMKF89B0-C5
Polarity Swapped
Lane Swapped
Lane/Polarity Swapped
Polarity Swapped
90_MIPI_AP_TO_DISPLAY_CLK_N
90_MIPI_AP_TO_DISPLAY_CLK_P
90_MIPI_AP_TO_DISPLAY_D0_P
90_MIPI_AP_TO_DISPLAY_D0_N
90_MIPI_AP_TO_DISPLAY_D2_P
90_MIPI_AP_TO_DISPLAY_D2_N
90_MIPI_AP_TO_DISPLAY_D1_N
90_MIPI_AP_TO_DISPLAY_D1_P
90_MIPI_AP_TO_DISPLAY_D3_N
90_MIPI_AP_TO_DISPLAY_D3_P
ANALOG_MIPI_AP_REXT
R1300
200
1%
1/32W
MF
01005
RODM=SOC
NC_LPDP_AP_TX0P
NC_LPDP_AP_TX0N
NC_LPDP_AP_TX1P
NC_LPDP_AP_TX1N
NC_LPDP_AP_TX2P
NC_LPDP_AP_TX2N
NC_LPDP_AP_TX3P
NC_LPDP_AP_TX3N
NC_LPDP_AP_AUXP
NC_LPDP_AP_AUXN
NC_LPDP_AP_RCALP
NC_LPDP_AP_RCALN
MIPID_DPCLK
MIPID_DNCLK
MIPID_DPDATA0
MIPID_DNDATA0
MIPID_DPDATA1
MIPID_DNDATA1
MIPID_DPDATA2
MIPID_DNDATA2
MIPID_DPDATA3
MIPID_DNDATA3
MIPID_REXT
LPDP_TX0P
LPDP_TX0N
LPDP_TX1P
LPDP_TX1N
LPDP_TX2P
LPDP_TX2N
LPDP_TX3P
LPDP_TX3N
LPDP_AUX_P
LPDP_AUX_N
LPDP_RCAL_P
LPDP_RCAL_N
MIPI-D
LPDP-TX
DISP_I2C
DWI
GPIOS
DISP_I2C_SCL/DISP_SPMI_SCLK
DISP_I2C_SDA/DISP_SPMI_SDATA
DWI_CLK
DWI_DO
DISP_TOUCH_BSYNC0
DISP_TOUCH_BSYNC1
DISP_TOUCH_EB
DISP_POL
DISP_TE
DP_WAKEUP
EDP_HPD
NC_I2C_DISP_SCL
NC_I2C_DISP_SDA
NC_DWI_PMGR_TO_BACKLIGHT_CLK
NC_DWI_PMGR_TO_BACKLIGHT_DATA
NC_TOUCH_BSYNC0_DISP
NC_TOUCH_BSYNC1_DISP
NC_POL_DISP
IO_AP_FROM_DISPLAY_TE
NC_WAKEUP_DP_DISP
NC_EDP_HPD_DISP
DISPLAY_TE to provide WDG

SOC: AP Serial



SOC: AP GPIO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GPIO
GPIO[0-8]: 1.2V
56 NC_AP_GPIO0 L3 GPIO0/I2C5_SCL
56 NC_AP_GPIO1 L2 GPIO1/I2C5_SDA
56 NC_AP_GPIO2 N4 GPIO2
56 GPIO_AP_FROM_WLAN_TIME_SYNC_1V2 N3 GPIO3
56 GPIO_AP_TO_BB_COREDUMP_1V2 N2 GPIO4
56 GPIO_AP_FROM_BB_RESET_DETECT_1V2_L P4 GPIO5
56 NC_AP_GPIO6 P2 GPIO6
56 NC_AP_GPIO7 T4 GPIO7
56 NC_AP_GPIO8 T3 GPIO8
56 GPIO_BOARD_REV3 P64 GPIO9
56 GPIO_BOARD_REV2 AP65 GPIO10
56 GPIO_BOARD_REV1 AP64 GPIO11
56 GPIO_BOARD_REV0 B47 GPIO12
56 GPIO_AP_CANARY1 AW64 GPIO13
56 GPIO_AP_CANARY2 AW66 GPIO14
56 GPIO_AP_BI_CCG2_SWDIO AM65 GPIO15
GPIO16 AU64 GPIO_AP_TO_CCG2_SWCLK 56
GPIO17 AU65 NC_AP_GPIO17 56
GPIO18 BY66 GPIO_AP_FROM_DISPLAY_PANEL_ID 56
GPIO19 AD64 PP1V8_IO PMU_ID: AVUS=1, WHITNEY = NC
GPIO20 AB65 NC_AP_GPIO20 56
GPIO21 BY64 NC_AP_GPIO21 56
GPIO22 BY65 GPIO_AP_TO_NFC_DEV_WAKE 56
GPIO23 AU66 NC_AP_GPIO23 56
GPIO24 AT64 GPIO_AP_FROM_CODEC_INT_L 56
GPIO25 BW66 GPIO_AP_FROM_SPKRAMP_TOP_INT_L 56
GPIO26 BU64 GPIO_AP_TO_SPKRAMP_TOP_RESET_L 56
GPIO27 BU65 GPIO_AP_FROM_BT_AUDIO_SYNC 56
GPIO28 BU66 GPIO_AP_TO_AMUX_PMU_SYNC 56
GPIO29 P66 GPIO_AP_TO_TOUCH_RESET_L 56
GPIO30 P65 NC_AP_GPIO30 56
GPIO31 AM64 NC_AP_GPIO31 56

SOC: AOP

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Signal	Pin	Function
I2C0_AOP_SCL	CP36	AOP_I2CM0_SCL
I2C0_AOP_SDA	CJ32	AOP_I2CM0_SDA
I2C1_AOP_SCL	CM34	AOP_I2CM1_SCL
I2C1_AOP_SDA	CM26	AOP_I2CM1_SDA
SPI0_AOP_FROM_IMU_R1_MISO	CJ30	AOP_SPI0_MISO
SPI0_AOP_TO_IMU_R1_MOSI	CK23	AOP_SPI0_MOSI
SPI0_AOP_TO_IMU_R1_SCLK_R	CK30	AOP_SPI0_SCLK
NC_SPI1_AOP_MISO	CJ42	AOP_SPI1_MISO
NC_SPI1_AOP_MOSI	CL42	AOP_SPI1_MOSI
NC_SPI1_AOP_SCLK	CL55	AOP_SPI1_SCLK
I2S0_AOP_FROM_CODEC_ASP1_DIN	CK53	AOP_I2S0_DIN
I2S0_AOP_TO_CODEC_ASP1_DOUT	CL53	AOP_I2S0_DOUT
I2S0_AOP_FROM_CODEC_ASP1_BCLK	CK40	AOP_I2S0_BCLK
I2S0_AOP_FROM_CODEC_ASP1_LRCLK	CK51	AOP_I2S0_LRCK
I2S0_AOP_TO_CODEC_MCLK1_R	CM42	AOP_I2S0_MCK/AOP_PDM_CLK2
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN	CL40	AOP_I2S1_DIN
I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT	CM61	AOP_I2S1_DOUT/AOP_PDM_IN2_DAT
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK_R	CM40	AOP_I2S1_BCLK/AOP_PDM_IN1_CLK
I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK_R	CM62	AOP_I2S1_LRCK/AOP_PDM_IN2_CLK
I2S1_AOP_TO_SPKRAMP_BOT_ARC_MCLK	CJ40	AOP_I2S1_MCK
SPMI1_AOP_BI_RF_DATA	CM24	AOP_UART0_RXD/NUB_SPMI1_SDATA
SPMI1_AOP_TO_RF_CLK	CM32	AOP_UART0_TXD/NUB_SPMI1_SCLK
UART1_AOP_FROM_TOUCH_RXD	CK7	AOP_UART1_RXD/NUB_SPMI2_SDATA
UART1_AOP_TO_TOUCH_TXD	CL32	AOP_UART1_TXD/NUB_SPMI2_SCLK
UART2_AOP_FROM_BB_RXD	CL61	AOP_UART2_RXD
UART2_AOP_TO_BB_TXD	CR36	AOP_UART2_TXD

Signal	Pin	Function
GPIO_AOP_FROM_IMU_DATARDY	CL62	AOP_FUNC0
GPIO_AOP_TO_IMU_SPI_CS_L	CL34	AOP_FUNC1
GPIO_AOP_FROM_PEARL_B2B_DETECT	CM63	AOP_FUNC2
GPIO_AOP_TO_R1_SPI_CS_L	CJ34	AOP_FUNC3
GPIO_AOP_FROM_R1_INT	CK34	AOP_FUNC4
GPIO_AOP_TO_R1_COREDUMP_TRIGGER	CM55	AOP_FUNC5
GPIO_AOP_TO_R1_TIME_SYNC	CR38	AOP_FUNC6
GPIO_AOP_TO_CODEC_RESET_L	CM53	AOP_FUNC7
GPIO_AOP_TO_CODEC_CLP_EN	CP38	AOP_FUNC8
GPIO_AOP_FROM_IRCAM_B2B_DETECT	CM51	AOP_FUNC9/AOP_LPPLL
GPIO_AOP_FROM_NFC_HOST_WAKE	CM36	AOP_FUNC10
GPIO_AOP_FROM_SPKAMP_BOT_ARC_INT_L	CM47	AOP_FUNC11
GPIO_AOP_TO_WLAN_CONTEXT_A	CL36	AOP_FUNC12
GPIO_AOP_TO_WLAN_CONTEXT_B	CL64	AOP_FUNC13
GPIO_AOP_FROM_TOUCH_CTS	CJ36	AOP_FUNC14
GPIO_AOP_BI_PROX_INT_L	CK57	AOP_FUNC15/AOP_PDM_CLK4
GPIO_AOP_FROM_ALS_INT_L	CK36	AOP_FUNC16/AOP_PDM_CLK3
GPIO_AOP_FROM_K2_INT_L	CM64	AOP_FUNC17
GPIO_AOP_FROM_COMPASS_INT	CM38	AOP_FUNC18
GPIO_AOP_FROM_HALL_CASE_INT_L	CM59	AOP_FUNC19
GPIO_AOP_FROM_HALL_FLAP_INT_L	CL38	AOP_FUNC20
GPIO_AOP_TO_TOUCH_INT_L	CJ61	AOP_FUNC21
GPIO_AOP_TOUCH_FROM_DISPLAY_BSYNC1	CJ38	AOP_FUNC22

SPI0_AOP_TO_IMU_R1_SCLK — R1601 33.2 1% 1/32W MF 01005 ROOM=SOC

I2S0_AOP_TO_CODEC_MCLK1 — R1603 33.2 1% 1/32W MF 01005 ROOM=SOC

I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK — R1604 49.9 1% 1/32W MF 01005 ROOM=SOC

I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK — R1605 49.9 1% 1/32W MF 01005 ROOM=SOC

C1607 15PF 5% 25V NP0-C0G 01005-1 ROOM=B2B_INTERPOSER NOSTUFF

SOC: SMC

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Signal	Pin	Function
I2C0_SMC_SCL	CL23	SMC_I2CM0_SCL
I2C0_SMC_SDA	CM30	SMC_I2CM0_SDA
I2C1_SMC_SCL	CL30	SMC_I2CM1_SCL/SMC_UART1_TXD
I2C1_SMC_SDA	CJ6	SMC_I2CM1_SDA/SMC_UART1_RXD
I2C2_SMC_SDA	CJ28	SMC_UART0_RXD/SMC_I2CM2_SDA
I2C2_SMC_SCL	CL24	SMC_UART0_TXD/SMC_I2CM2_SCL

SOC: NUB

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Signal	Pin	Function	Group
SPMI0_NUB_TO_PMU_DOTARA_CLK_R	CJ9	NUB_SPMI0_SCLK	SPMI
SPMI0_NUB_BI_PMU_DOTARA_DATA_R	CL26	NUB_SPMI0_SDATA	SPMI
SWD_NUB_TO_MANY_SWCLK	CJ21	NUB_SWD_TCK_OUT	SWD
SWD_NUB_BI_PMU_SWDIO	CJ24	NUB_SWD_TMS0	SWD
SWD_NUB_BI_R1_SWDIO	CJ19	NUB_SWD_TMS1	SWD
IO_HYDRA_TO_NUB_PMU_DOCK_CONNECT	CK24	NUB_DOCK_CONNECT	DOCK
IO_HYDRA_TO_NUB_DOCK_ATTENTION	CJ15	NUB_DOCK_ATTENTION/NUB_PDM_CLK1	DOCK
GPIO_NUB_FROM_CCG2_INT_L	CJ26	NUB_GPIO_0/AOP_PDM_CLK0	GPIO
GPIO_NUB_FROM_GECKO_IRQ_L	CK9	NUB_GPIO_1/AOP_PDM_DATA0	GPIO
GPIO_NUB_TO_GECKO_RESET_L	CM28	NUB_GPIO_2/AOP_FUNC_23	GPIO
NC_NUB_GPIO3_AP	CJ7	NUB_GPIO_3	GPIO
GPIO_NUB_TO_BBPMU_CLK_EN (CLK_DATA_CON)	CL28	NUB_GPIO_4/AOP_PDM_DATA1	GPIO
NC_NUB_GPIO5_AP (NO_TEST=1)	CJ11	NUB_GPIO_5/AOP_PDM_DATAOUT	GPIO
NC_NUB_GPIO6_AP (NO_TEST=1)	CK28	NUB_GPIO_6/AOP_PDM_OUT0_CLK	GPIO
SWD_DOCK_TO_AP_SWCLK	CJ55	JTAG_TCK	JTAG
SWD_DOCK_BI_AP_SWDIO	CJ44	JTAG_TMS	JTAG
	CL44	JTAG_SEL	JTAG
	CJ62	JTAG_TDI	JTAG
	CK62	JTAG_TDO	JTAG
	CL51	JTAG_TRST*	JTAG
90_USB_DBG_DATA_N	CR42	DBG_USB_DM	DEBUG USB
90_USB_DBG_DATA_P	CP42	DBG_USB_DP	DEBUG USB
	CK45	DBG_USB_ID	DEBUG USB
ANALOG_DBG_USB_VBUS_REXT	CM45	DBG_USB_REXT	DEBUG USB
PP3V3_USB_DEBUG_FILT	CL45	DBG_USB_VBUS	DEBUG USB
NC_CLK_CLK24M_OUT	CJ23	CLK24M_OUT	MISC
IO_PMU_TO_SYSTEM_RESET_L	CK42	COLD_RESET*	MISC
	CJ57	CFSB_AON	MISC
CLK_PMU_TO_AOP_32K	CL63	RT_CLK32768	MISC
IO_AP_TO_PMU_RESET	CL59	WDOG	MISC
PROBE_AOP_TO_DDR_SLEEP1	CM44	AON_SLEEP1_RESET*	MISC
	CJ3	LP4_IN_RESET*	MISC

SPMI0_NUB_TO_PMU_DOTARA_CLK — R1610 0.00 0% 1/32W MF 01005 ROOM=SOC

SPMI0_NUB_BI_PMU_DOTARA_DATA — R1611 61.9 1% 1/32W MF 01005 ROOM=SOC 118S0755

R1620 200 1% 1/32W MF 01005 ROOM=SOC

SOC: CPU/GPU

1.029V @ 15.2A MAX
0.909V @ 15.2A MAX
0.540V @ 3.8A MAX
PP_CPU_PCORE

C1702 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1703 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1704 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1705 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1706 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1707 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT

C1708 26UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1709 26UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE

0.970V @ 3.6A MAX
0.650V @ 2.1A MAX
0.530V @ 1.2A MAX
PP_CPU_ECORE

C1791 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1792 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1794 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

ANALOG_CPU_PCORE_SENSEP

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CPU/GPU

AN46	VDD_PCPU	VDD_GPU	AA29
AN50	VDD_PCPU	VDD_GPU	AA37
AN54	VDD_PCPU	VDD_GPU	AA46
AN58	VDD_PCPU	VDD_GPU	AA54
AR43	VDD_PCPU	VDD_GPU	AC27
AR48	VDD_PCPU	VDD_GPU	AC31
AR56	VDD_PCPU	VDD_GPU	AC35
AV41	VDD_PCPU	VDD_GPU	W56
AV58	VDD_PCPU	VDD_GPU	AC39
BB58	VDD_PCPU	VDD_GPU	F27
BF41	VDD_PCPU	VDD_GPU	F31
BK41	VDD_PCPU	VDD_GPU	F35
BK54	VDD_PCPU	VDD_GPU	F48
BK58	VDD_PCPU	VDD_GPU	F52
BM43	VDD_PCPU	VDD_GPU	H33
BM48	VDD_PCPU	VDD_GPU	H41
BM52	VDD_PCPU	VDD_GPU	H50
BM56	VDD_PCPU	VDD_GPU	K27
BP46	VDD_PCPU	VDD_GPU	K31
BP50	VDD_PCPU	VDD_GPU	K35
BT56	VDD_PCPU	VDD_GPU	K39
CC46	VDD_PCPU	VDD_GPU	K43
CC50	VDD_PCPU	VDD_GPU	K48
CC56	VDD_PCPU	VDD_GPU	K52
BM39	VDD_PCPU_SENSE	VDD_GPU	K56
		VDD_GPU	M29
AN29	VDD_ECPU	VDD_GPU	M46
AN33	VDD_ECPU	VDD_GPU	M54
AN37	VDD_ECPU	VDD_GPU	R27
AR27	VDD_ECPU	VDD_GPU	R31
AR31	VDD_ECPU	VDD_GPU	R35
AR35	VDD_ECPU	VDD_GPU	R48
AR39	VDD_ECPU	VDD_GPU	R52
AV33	VDD_ECPU	VDD_GPU	R56
AV37	VDD_ECPU	VDD_GPU	U33
AY27	VDD_ECPU	VDD_GPU	U50
AY39	VDD_ECPU	VDD_GPU	W27
BB29	VDD_ECPU	VDD_GPU	W31
BD27	VDD_ECPU	VDD_GPU	W35
BF29	VDD_ECPU	VDD_GPU	W39
BF37	VDD_ECPU	VDD_GPU	W43
BH27	VDD_ECPU	VDD_GPU	W48
BH35	VDD_ECPU	VDD_GPU	W52
BK29	VDD_ECPU	VDD_GPU_SENSE	AE27
BK33	VDD_ECPU		
BK37	VDD_ECPU		

0.985V @ 12.6A MAX
0.686V @ 5.80A MAX
0.562V @ 3.20A MAX
PP_GPU

C1730 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1731 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1733 26UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1734 15UF 20% 4V X5R-CERM 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1735 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1736 26UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE

ANALOG_GPU_SENSEP

SOC: SRAM

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SRAM

AR52	VDD_SRAM_PCPU	VDD_SRAM_SOC	AA18
BB41	VDD_SRAM_PCPU	VDD_SRAM_SOC	AA58
BF58	VDD_SRAM_PCPU	VDD_SRAM_SOC	AC12
BK46	VDD_SRAM_PCPU	VDD_SRAM_SOC	AC48
		VDD_SRAM_SOC	AE18
AV29	VDD_SRAM_ECPU	VDD_SRAM_SOC	AE41
BB37	VDD_SRAM_ECPU	VDD_SRAM_SOC	AE54
BH31	VDD_SRAM_ECPU	VDD_SRAM_SOC	AG12
		VDD_SRAM_SOC	AG25
		VDD_SRAM_SOC	AG35
AA33	VDD_SRAM_GPU	VDD_SRAM_SOC	AG48
AA50	VDD_SRAM_GPU	VDD_SRAM_SOC	AJ18
H29	VDD_SRAM_GPU	VDD_SRAM_SOC	AJ29
H37	VDD_SRAM_GPU	VDD_SRAM_SOC	AJ41
H46	VDD_SRAM_GPU	VDD_SRAM_SOC	AJ54
H54	VDD_SRAM_GPU	VDD_SRAM_SOC	AL12
M33	VDD_SRAM_GPU	VDD_SRAM_SOC	AL25
M50	VDD_SRAM_GPU	VDD_SRAM_SOC	AL35
U29	VDD_SRAM_GPU	VDD_SRAM_SOC	AN18
U46	VDD_SRAM_GPU	VDD_SRAM_SOC	AR12
U54	VDD_SRAM_GPU	VDD_SRAM_SOC	AR25
		VDD_SRAM_SOC	AV18
		VDD_SRAM_SOC	AY12
		VDD_SRAM_SOC	AY25
		VDD_SRAM_SOC	BB18
BP54	VDD_SRAM_ANE	VDD_SRAM_SOC	BD25
BV46	VDD_SRAM_ANE	VDD_SRAM_SOC	BF18
CC54	VDD_SRAM_ANE	VDD_SRAM_SOC	BK18
		VDD_SRAM_SOC	BM12
		VDD_SRAM_SOC	BM25
		VDD_SRAM_SOC	BM35
		VDD_SRAM_SOC	BP18
		VDD_SRAM_SOC	BP29
		VDD_SRAM_SOC	BP41
		VDD_SRAM_SOC	BT12
		VDD_SRAM_SOC	BT25
		VDD_SRAM_SOC	BT35
		VDD_SRAM_SOC	BV18
		VDD_SRAM_SOC	BV29
		VDD_SRAM_SOC	BV41
		VDD_SRAM_SOC	CA35
		VDD_SRAM_SOC	CE25
		VDD_SRAM_SOC	CE56
		VDD_SRAM_SOC	K20
		VDD_SRAM_SOC	R12
		VDD_SRAM_SOC	W20

0.752V @ 2.7A MAX
PP_SRAM_S1

C1772 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1773 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1774 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT

SOC: SOC

0.770V @ 4.9A MAX
0.651V @ 3.4A MAX
0.590V @ 2.7A MAX
PP_SOC_S1

C1760 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1761 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1765 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

C1762 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1763 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1764 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE

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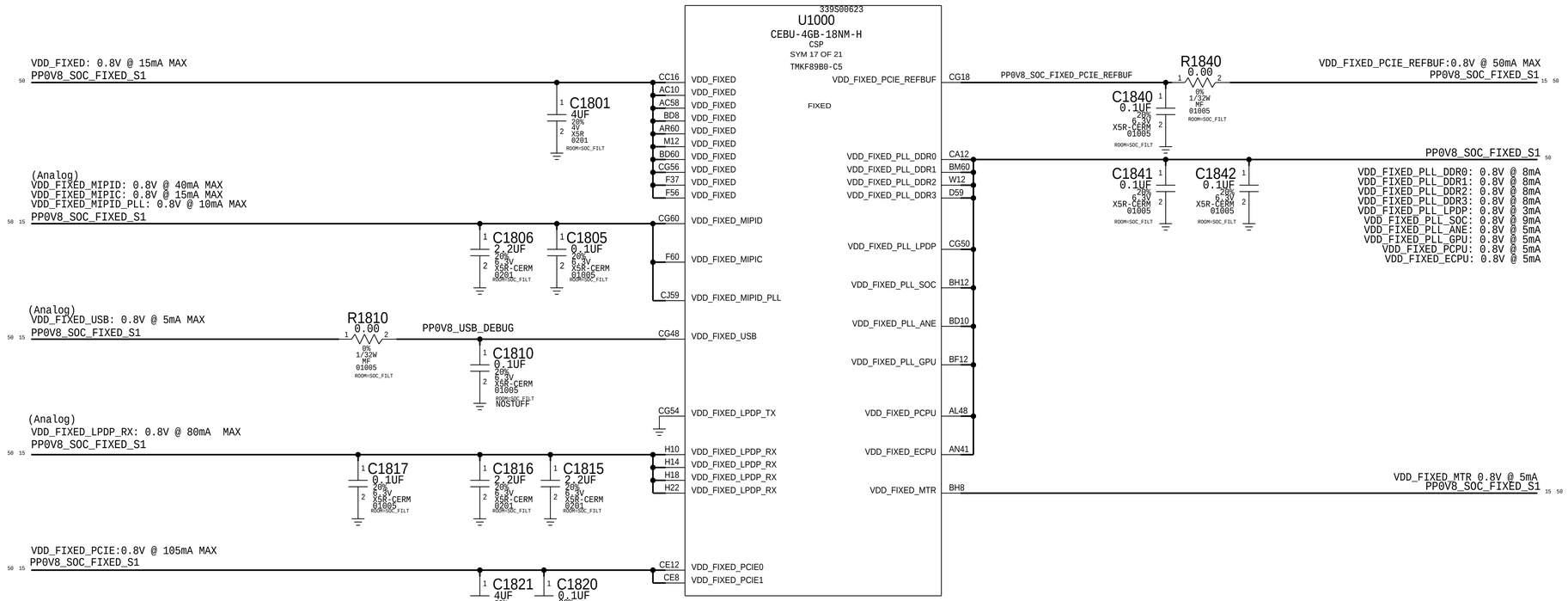
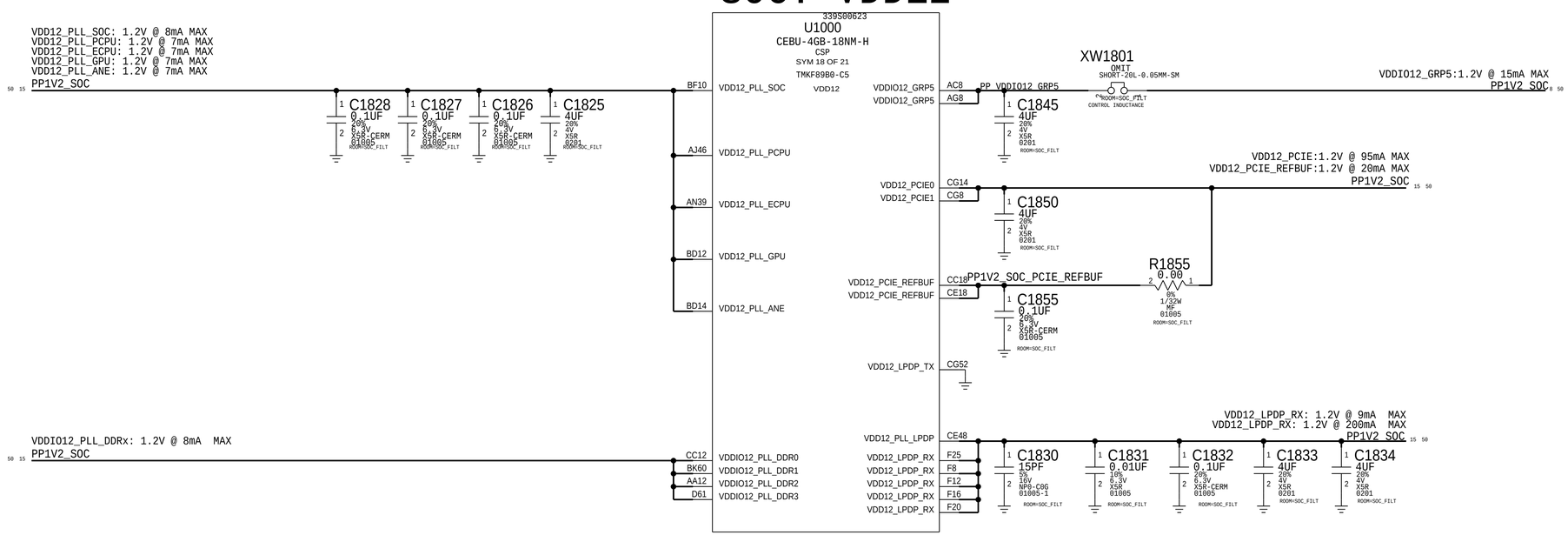
AA41	VDD_SOC	VDD_SOC	H25
AC43	VDD_SOC	VDD_SOC	BH25
AC52	VDD_SOC	VDD_SOC	BH39
AC56	VDD_SOC	VDD_SOC	BK10
AE8	VDD_SOC	VDD_SOC	BK14
AE22	VDD_SOC	VDD_SOC	BK22
AE33	VDD_SOC	VDD_SOC	BM16
AE37	VDD_SOC	VDD_SOC	BM20
AE46	VDD_SOC	VDD_SOC	BM27
AE50	VDD_SOC	VDD_SOC	BM31
AE58	VDD_SOC	VDD_SOC	BP14
AG20	VDD_SOC	VDD_SOC	BP22
AG27	VDD_SOC	VDD_SOC	BP33
AG31	VDD_SOC	VDD_SOC	BP37
AG39	VDD_SOC	VDD_SOC	BT16
AG43	VDD_SOC	VDD_SOC	BT20
AG52	VDD_SOC	VDD_SOC	BT27
AG56	VDD_SOC	VDD_SOC	BT31
AJ22	VDD_SOC	VDD_SOC	BT39
AJ33	VDD_SOC	VDD_SOC	BT43
AJ37	VDD_SOC	VDD_SOC	M56
AJ50	VDD_SOC	VDD_SOC	BV14
AJ58	VDD_SOC	VDD_SOC	BV22
AL20	VDD_SOC	VDD_SOC	BV33
AL27	VDD_SOC	VDD_SOC	BV37
AL31	VDD_SOC	VDD_SOC	BV56
AL39	VDD_SOC	VDD_SOC	CA16
AC20	VDD_SOC	VDD_SOC	CA20
AL43	VDD_SOC	VDD_SOC	CA27
AL52	VDD_SOC	VDD_SOC	CA31
AL56	VDD_SOC	VDD_SOC	CA39
AN10	VDD_SOC	VDD_SOC	CA43
AN14	VDD_SOC	VDD_SOC	CC14
AN22	VDD_SOC	VDD_SOC	CC22
AR16	VDD_SOC	VDD_SOC	CE20
AR20	VDD_SOC	VDD_SOC	CE27
AV10	VDD_SOC	VDD_SOC	AY16
AV14	VDD_SOC	VDD_SOC	CE52
AV22	VDD_SOC	VDD_SOC	CG22
BB10	VDD_SOC	VDD_SOC	F41
BB14	VDD_SOC	VDD_SOC	U12
BB22	VDD_SOC		
BB60	VDD_SOC		
BD16	VDD_SOC		
BD20	VDD_SOC		
BD39	VDD_SOC		
BF22	VDD_SOC		
BF8	VDD_SOC		
BF14	VDD_SOC		
BH16	VDD_SOC		
BH20	VDD_SOC		
		VDD_SOC_SENSE	AY20

ANALOG_SOC_SENSE_P

SOC: FIXED



SOC: VDD12



SOC: DDR

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DDR

0.895V @ 910mA MAX
0.735V @ 550mA MAX
0.614V @ 300mA MAX

PP_DCS_S1 (50)

C1989 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT
C1988 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1987 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1986 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1985 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

Place caps on SoC Corners

Pin	Signal
BP10	VDD_DCS_DDR0
CC10	VDD_DCS_DDR0
BP58	VDD_DCS_DDR1
CC58	VDD_DCS_DDR1
AA10	VDD_DCS_DDR2
K10	VDD_DCS_DDR2
H58	VDD_DCS_DDR3
W58	VDD_DCS_DDR3
A62	VDD_DCS_SENSE

ANALOG_DCS_SENSEP (OUT) (5)

VDDQL* TOTAL: 0.573V - 0.63V @ 620mA MAX
Place caps on SoC Corners

PP0V6_VDDQL_S1 (50 7)

C1994 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT
C1993 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1992 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1991 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1990 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

Pin	Signal
BG1	VDDQL_DDR0
BL1	VDDQL_DDR0
BM8	VDDQL_DDR0
BR1	VDDQL_DDR0
CC8	VDDQL_DDR0
CH1	VDDQL_DDR0
CK1	VDDQL_DDR0
CM1	VDDQL_DDR0
BE67	VDDQL_DDR1
BJ67	VDDQL_DDR1
BN67	VDDQL_DDR1
BP60	VDDQL_DDR1
CE60	VDDQL_DDR1
CF67	VDDQL_DDR1
CJ67	VDDQL_DDR1
CL67	VDDQL_DDR1
AF1	VDDQL_DDR2
AK1	VDDQL_DDR2
AP1	VDDQL_DDR2
E1	VDDQL_DDR2
J1	VDDQL_DDR2
K8	VDDQL_DDR2
N1	VDDQL_DDR2
W8	VDDQL_DDR2
AD67	VDDQL_DDR3
AH67	VDDQL_DDR3
AM67	VDDQL_DDR3
D67	VDDQL_DDR3
G67	VDDQL_DDR3
K60	VDDQL_DDR3
L67	VDDQL_DDR3
W60	VDDQL_DDR3
A64	VDDQL_SENSE

ANALOG_VDDQL_SENSEP (OUT) (5)

VDD2_DDR*: 1.06V - 1.17V @ 2.2A MAX
PP1V1_S2 (16 50)

C1980 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1981 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1982 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1983 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

Added C1982, C1983 (2.2uF for each VDD2_DDRx Channel)

Pin	Signal
BC2	VDD2_DDR0
BU1	VDD2_DDR0
BY1	VDD2_DDR0
CD1	VDD2_DDR0
CM3	VDD2_DDR0
BC66	VDD2_DDR1
BU67	VDD2_DDR1
BY67	VDD2_DDR1
CD67	VDD2_DDR1
CM65	VDD2_DDR1
AB1	VDD2_DDR2
AT2	VDD2_DDR2
D3	VDD2_DDR2
P1	VDD2_DDR2
V1	VDD2_DDR2
AB67	VDD2_DDR3
AT66	VDD2_DDR3
D65	VDD2_DDR3
P67	VDD2_DDR3
V67	VDD2_DDR3
CJ4	VDDIO11_RET_DDR0
CJ64	VDDIO11_RET_DDR1
D4	VDDIO11_RET_DDR2
D62	VDDIO11_RET_DDR3

PP1V1_S2 (16 50)
Current included in VDD2

VDD1_DDR*: 1.70V - 1.95V @ 220mA MAX
PP1V8_S2 (50)

C1996 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT
C1997 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT
C1998 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT
C1999 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT

Pin	Signal
BC1	VDD1_DDR0
CN2	VDD1_DDR0
BC67	VDD1_DDR1
CN66	VDD1_DDR1
AT1	VDD1_DDR2
C2	VDD1_DDR2
AT67	VDD1_DDR3
C66	VDD1_DDR3

SOC: AOP/AVE/ISP/USB

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AOP/AVE/DISP/USB

VDD_LOW: 0.71V @ 220mA MAX
VDD_LOW_FLPPLL: 0.71V @ 0.3mA MAX
VDD_LOW_ULPPLL: 0.71V @ 0.03mA MAX
VDD_LOW_USB_DEBUGL: 0.71V @ 5mA MAX

PP0V7_VDD_LOW_S2 (50)

C1900 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

Pin	Signal
CC29	VDD_LOW
CC33	VDD_LOW
CC37	VDD_LOW
CC41	VDD_LOW
CE35	VDD_LOW
CE39	VDD_LOW
CE43	VDD_LOW
CG25	VDD_LOW

R1905 10 5% 1/32W MF 01005 ROOM=SOC_FILT
C1905 0.47UF 20% 6.3V X6R 01005-1 ROOM=SOC_FILT
PP0V7_VDD_LOW_FLPPLL_R — CE33 VDD_LOW_FLPPLL

R1910 100 5% 1/32W MF 01005 ROOM=SOC_FILT
C1910 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
PP0V7_VDD_LOW_ULPPLL_R — CE31 VDD_LOW_ULPPLL

R1920 0.00 0% 1/32W MF 01005 ROOM=SOC_FILT
C1920 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
PP_VDD_LOW_USB_DEBUG — CG46 VDD_LOW_USB_DEBUG

PP_AVE_S1 (50)

C1927 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1926 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1925 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE

Pin	Signal
AA22	VDD_AVE
AC25	VDD_AVE
K12	VDD_AVE
K16	VDD_AVE
K25	VDD_AVE
M14	VDD_AVE
R25	VDD_AVE
U14	VDD_AVE
W16	VDD_AVE
W25	VDD_AVE

VDD_AVE: 0.59V - 0.801V @ 3.2A MAX
VDD_DISP: 0.56V - 0.718V @ 1.5A MAX

PP_DISP_S1 (50)

C1931 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT
C1930 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT

Pin	Signal
AA14	VDD_DISP
AC16	VDD_DISP
AE10	VDD_DISP
AE14	VDD_DISP
AG16	VDD_DISP
AJ10	VDD_DISP
AJ14	VDD_DISP
AL16	VDD_DISP

VDD33_USB*: 3.3V @ 15mA MAX

PP3V3_USB (50) — CK47 VDD33_USB

PP3V3_USB_DEBUG (21) — R1940 0.00 0% 1/32W MF 01005 ROOM=SOC_FILT

PP3V3_USB_DEBUG_FILT (13) — CJ47 VDD33_USB_DEBUG

C1935 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1940 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

VDD18_TSADC_SOC: 1.8V @ 3mA MAX
VDD18_TSADC_CPU: 1.8V @ 5mA MAX
VDD18_TSADC_CPU: 1.8V @ 3mA MAX
VDD18_AMUX: 1.8V @ 0.3mA MAX
PP1V8_IO (16 50)

Pin	Signal
BP25	VDD18_TSADC_SOC0
CJ51	VDD18_TSADC_SOC1
C4	VDD18_TSADC_SOC2
AV39	VDD18_TSADC_CPU0
AR41	VDD18_TSADC_CPU1
BK50	VDD18_TSADC_CPU2
BK52	VDD18_TSADC_CPU3
AL46	VDD18_TSADC_CPU4
F46	VDD18_TSADC_GPU0
BW4	VDD18_AMUX
CJ49	VDD18_USB
CJ17	VDD18_XTAL

VDD18_USB: 1.8V @ 20mA MAX
VDD18_XTAL: 1.8V @ 1mA MAX
PP1V8_IO (16 50)

FL1950 2400HM-25%-0.2A-0.90HM 01005 ROOM=SOC_FILT
PP1V8_XTAL

C1945 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1950 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1946 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

VDDIO18_AOP: 1.8 @ 20mA MAX
PP1V8_S2 (16 29 46 49 50 54)

Pin	Signal
CG29	VDDIO18_AOP
CG33	VDDIO18_AOP
CG37	VDDIO18_AOP
CG39	VDDIO18_AOP
CG41	VDDIO18_AOP

C1960 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1961 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

VDD18_MIPIC:1.8 @ 2mA MAX
VDD18_MIPID:1.8 @ 20mA MAX
PP1V8_IO (50)

Pin	Signal
F58	VDD18_MIPIC
CG58	VDD18_MIPID
AC60	VDD18_EFUSE1
CA25	VDD18_EFUSE2

C1965 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1966 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

VDDIO18_GPR*: 1.8V @ 75mA MAX
VDDIO18_MTR: 1.8V @ 28mA MAX
PP1V8_IO (50)

Pin	Signal
AL8	VDDIO18_GRP1
AR8	VDDIO18_GRP1
AY8	VDDIO18_GRP1
AG60	VDDIO18_GRP3
AL60	VDDIO18_GRP3
AN60	VDDIO18_GRP3
AY60	VDDIO18_GRP3
BH60	VDDIO18_GRP3
F39	VDDIO18_GRP4
F43	VDDIO18_GRP4
BK8	VDDIO18_MTR

C1970 26UF 20% 6.3V X5R 0402-0.1MM ROOM=SOC_FILT OMIT_TABLE
C1971 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1972 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1973 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

VDDIO18_ULPLL: 1.8V @ 0.03mA MAX
PP1V8_S2 (16 29 46 49 50 54)

VDD18_ULPPLL (CE29) — PP1V8_ULPPLL_R — R1975 100 5% 1/32W MF 01005 ROOM=SOC_FILT

C1975 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

VDDIO18_FMON: 1.8V @ 0.1mA MAX
PP1V8_IO (16 50)

VDD18_FMON (BV25) — PP1V8_FMON_R — R1976 49.9 1% 1/32W MF 01005

C1976 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

SOC: GND

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A11	VSS	VSS	AL54
A15	VSS	VSS	AL58
A19	VSS	VSS	AM1
A2	VSS	VSS	AM3
A23	VSS	VSS	AN12
A26	VSS	VSS	AN16
A3	VSS	VSS	AN20
A30	VSS	VSS	AN25
A34	VSS	VSS	AN27
A36	VSS	VSS	AN31
A38	VSS	VSS	AN35
A4	VSS	VSS	AN43
A5	VSS	VSS	AN48
A51	VSS	VSS	AN52
A53	VSS	VSS	AN56
A61	VSS	VSS	AN8
A65	VSS	VSS	AP67
A66	VSS	VSS	AR10
A7	VSS	VSS	AR14
AA16	VSS	VSS	AR18
AA20	VSS	VSS	AR22
AA25	VSS	VSS	AR29
AA27	VSS	VSS	AR33
AA31	VSS	VSS	AR37
AA35	VSS	VSS	AR46
AA39	VSS	VSS	AR50
AA43	VSS	VSS	AR54
AA48	VSS	VSS	AR58
AA52	VSS	VSS	AT65
AA56	VSS	VSS	AU1
AA60	VSS	VSS	AU3
AA8	VSS	VSS	AU67
AB64	VSS	VSS	AV12
AC14	VSS	VSS	AV16
AC18	VSS	VSS	AV20
AC22	VSS	VSS	AV25
AC29	VSS	VSS	AV27
AC33	VSS	VSS	AV31
AC37	VSS	VSS	AV35
AC41	VSS	VSS	AV60
AC46	VSS	VSS	AV8
AC50	VSS	VSS	AW1
AC54	VSS	VSS	AW67
AD1	VSS	VSS	AY10
AD65	VSS	VSS	AY14
AE12	VSS	VSS	AY22
AE16	VSS	VSS	AY29
AE20	VSS	VSS	AY37
AE25	VSS	VSS	AY41
AE31	VSS	VSS	AY58
AE35	VSS	VSS	B1
AE39	VSS	VSS	B19
AE43	VSS	VSS	B2
AE48	VSS	VSS	B3
AE52	VSS	VSS	B34
AE56	VSS	VSS	B36
AE60	VSS	VSS	B38
AF3	VSS	VSS	B4
AF67	VSS	VSS	B42
AG10	VSS	VSS	B45
AG14	VSS	VSS	B5
AG18	VSS	VSS	B51
AG22	VSS	VSS	B53
AG29	VSS	VSS	B61
AG33	VSS	VSS	B62
AG37	VSS	VSS	B63
AG41	VSS	VSS	B64
AG46	VSS	VSS	B65
AG50	VSS	VSS	B66
AG54	VSS	VSS	B67
AG58	VSS	VSS	BA1
AH1	VSS	VSS	BA65
AH4	VSS	VSS	BA67
AJ12	VSS	VSS	BB12
AJ16	VSS	VSS	BB16
AJ20	VSS	VSS	BB20
AJ25	VSS	VSS	BB25
AJ27	VSS	VSS	BB27
AJ31	VSS	VSS	BB39
AJ35	VSS	VSS	BB8
AJ39	VSS	VSS	BC3
AJ43	VSS	VSS	BD18
AJ48	VSS	VSS	BD22
AJ52	VSS	VSS	BD29
AJ56	VSS	VSS	BD37
AJ60	VSS	VSS	BD41
AJ8	VSS	VSS	BD58
AK65	VSS	VSS	BE1
AK67	VSS	VSS	BE4
AL10	VSS	VSS	BF16
AL14	VSS	VSS	BF20
AL18	VSS	VSS	BF25
AL22	VSS	VSS	BF27
AL29	VSS	VSS	BF39
AL33	VSS	VSS	BF60
AL37	VSS	VSS	BG65
AL41	VSS	VSS	BG67
AL50	VSS	VSS	BH10

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BH14	VSS	VSS	CA29
BH18	VSS	VSS	CA33
BH22	VSS	VSS	CA37
BH29	VSS	VSS	CA41
BH33	VSS	VSS	CA46
BH37	VSS	VSS	CA56
BH41	VSS	VSS	CB1
BH58	VSS	VSS	CB4
BJ1	VSS	VSS	CB67
BJ3	VSS	VSS	CC20
BK12	VSS	VSS	CC25
BK16	VSS	VSS	CC27
BK20	VSS	VSS	CC31
BK25	VSS	VSS	CC35
BK27	VSS	VSS	CC39
BK31	VSS	VSS	CC43
BK35	VSS	VSS	CC48
BK39	VSS	VSS	CC52
BK43	VSS	VSS	CC60
BK48	VSS	VSS	CD2
BK56	VSS	VSS	CD65
BL67	VSS	VSS	CE10
BM10	VSS	VSS	CE14
BM14	VSS	VSS	CE22
BM18	VSS	VSS	CE37
BM22	VSS	VSS	CE41
BM29	VSS	VSS	CE46
BM33	VSS	VSS	CE50
BM37	VSS	VSS	CE54
BM41	VSS	VSS	CE58
BM46	VSS	VSS	CF1
BM50	VSS	VSS	CF4
BM54	VSS	VSS	CG12
BM58	VSS	VSS	CG16
BN1	VSS	VSS	CG20
BN65	VSS	VSS	CG27
BP12	VSS	VSS	CG31
BP16	VSS	VSS	CG35
BP20	VSS	VSS	CG43
BP27	VSS	VSS	CH2
BP31	VSS	VSS	CH3
BP35	VSS	VSS	CH4
BP43	VSS	VSS	CH64
BP48	VSS	VSS	CH65
BP52	VSS	VSS	CH66
BP56	VSS	VSS	CH67
BP8	VSS	VSS	CJ1
BR3	VSS	VSS	CJ13
BR64	VSS	VSS	CJ2
BR67	VSS	VSS	CJ45
BT14	VSS	VSS	CJ5
BT18	VSS	VSS	CJ53
BT22	VSS	VSS	CJ63
BT29	VSS	VSS	CJ66
BT33	VSS	VSS	CK11
BT37	VSS	VSS	CK15
BT41	VSS	VSS	CK17
BT46	VSS	VSS	CK19
BV12	VSS	VSS	CK2
BV16	VSS	VSS	CK21
BV20	VSS	VSS	CK26
BV27	VSS	VSS	CK32
BV31	VSS	VSS	CK38
BV35	VSS	VSS	CK4
BV39	VSS	VSS	CK44
BV43	VSS	VSS	CK49
BW1	VSS	VSS	CK5
BW65	VSS	VSS	CK55
BW67	VSS	VSS	CK6
BY2	VSS	VSS	CK61
BY3	VSS	VSS	CK63
BY4	VSS	VSS	CK64
C1	VSS	VSS	CK65
C13	VSS	VSS	CK66
C17	VSS	VSS	CK67
C21	VSS	VSS	CL1
C24	VSS	VSS	CL11
C28	VSS	VSS	CL15
C32	VSS	VSS	CL17
C36	VSS	VSS	CL19
C38	VSS	VSS	CL2
C5	VSS	VSS	CL21
C51	VSS	VSS	CL3
C53	VSS	VSS	CL4
C55	VSS	VSS	CL5
C57	VSS	VSS	CL6
C59	VSS	VSS	CL65
C6	VSS	VSS	CL66
C61	VSS	VSS	CL7
C62	VSS	VSS	CL9
C63	VSS	VSS	CM13
C64	VSS	VSS	CM17
C65	VSS	VSS	CM2
C67	VSS	VSS	CM21
C9	VSS	VSS	CM23
CA14	VSS	VSS	CM4
CA18	VSS	VSS	CM6
CA22	VSS	VSS	CM66

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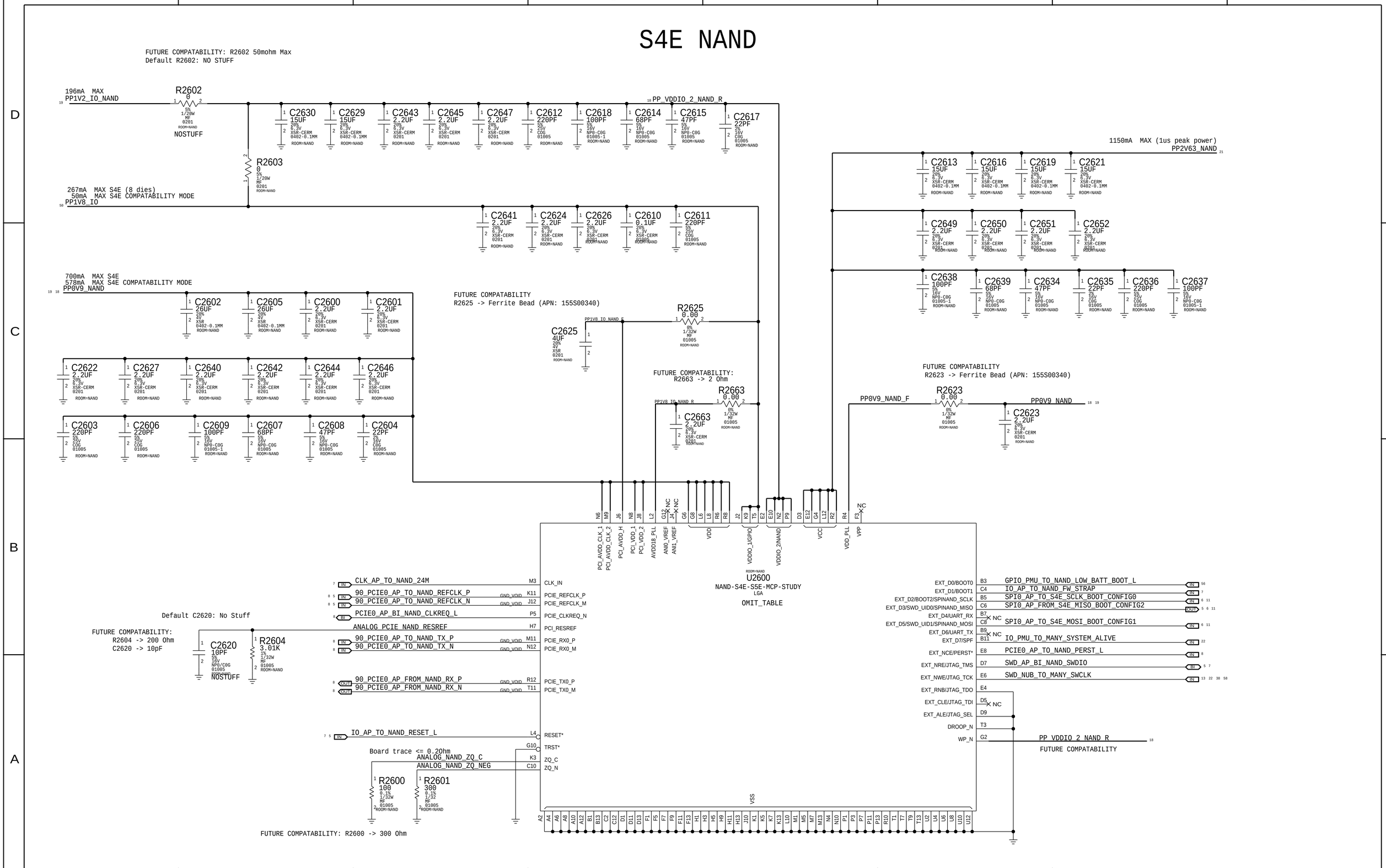
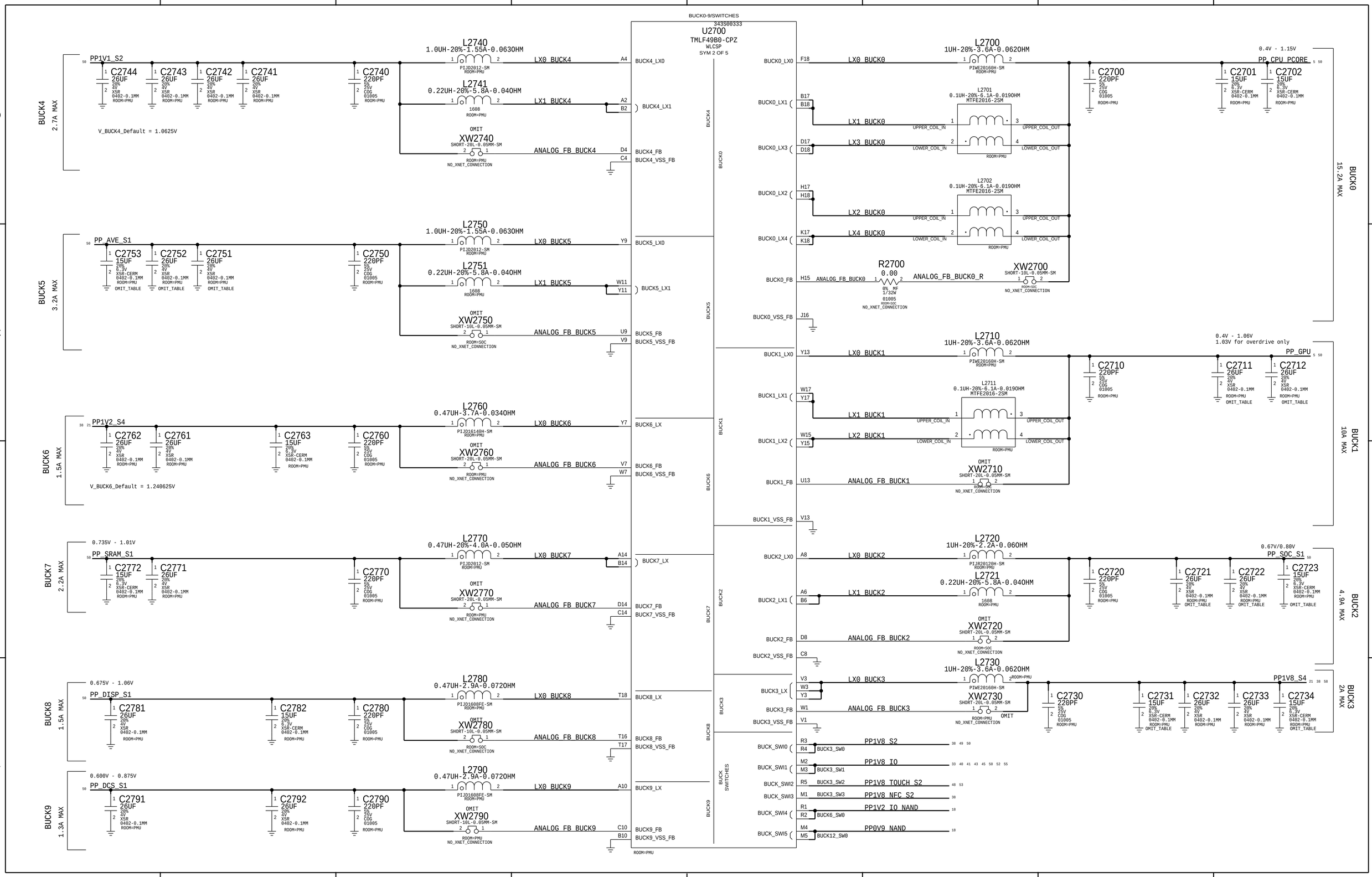
CM67	VSS	VSS	F10
CM9	VSS	VSS	F14
CN1	VSS	VSS	F18
CN13	VSS	VSS	F22
CN17	VSS	VSS	F29
CN21	VSS	VSS	F33
CN23	VSS	VSS	F50
CN24	VSS	VSS	F54
CN26	VSS	VSS	G1
CN28	VSS	VSS	G65
CN3	VSS	VSS	H12
CN30	VSS	VSS	H16
CN32	VSS	VSS	H20
CN34	VSS	VSS	H27
CN36	VSS	VSS	H31
CN38	VSS	VSS	H35
CN4	VSS	VSS	H39
CN40	VSS	VSS	H43
CN42	VSS	VSS	H48
CN44	VSS	VSS	H52
CN45	VSS	VSS	H56
CN47	VSS	VSS	H60
CN49	VSS	VSS	H8
CN51	VSS	VSS	J3
CN53	VSS	VSS	J67
CN55	VSS	VSS	K14
CN57	VSS	VSS	K18
CN59	VSS	VSS	K22
CN6	VSS	VSS	K29
CN61	VSS	VSS	K33
CN62	VSS	VSS	K37
CN63	VSS	VSS	K41
CN64	VSS	VSS	K46
CN65	VSS	VSS	K50
CN67	VSS	VSS	K54
CN9	VSS	VSS	K58
CP1	VSS	VSS	L1
CP11	VSS	VSS	M25
CP15	VSS	VSS	M27
CP19	VSS	VSS	M31
CP2	VSS	VSS	M35
CP23	VSS	VSS	M48
CP3	VSS	VSS	M52
CP34	VSS	VSS	N65
CP40	VSS	VSS	N67
CP45	VSS	VSS	P3
CP5	VSS	VSS	R14
CP57	VSS	VSS	R29
CP65	VSS	VSS	R33
CP66	VSS	VSS	R46
CP67	VSS	VSS	R50
CP7	VSS	VSS	R54
CR11	VSS	VSS	T1
CR15	VSS	VSS	T67
CR19	VSS	VSS	U25
CR2	VSS	VSS	U27
CR23	VSS	VSS	U31
CR3	VSS	VSS	U35
CR34	VSS	VSS	U48
CR40	VSS	VSS	U52
CR45	VSS	VSS	U56
CR5	VSS	VSS	V65
CR57	VSS	VSS	W10
CR65	VSS	VSS	W14
CR66	VSS	VSS	W18
CR7	VSS	VSS	W22
D1	VSS	VSS	W29
D11	VSS	VSS	W33
D15	VSS	VSS	W37
D2	VSS	VSS	W41
D23	VSS	VSS	W46
D26	VSS	VSS	W50
D30	VSS	VSS	W54
D36	VSS	VSS	Y1
D38	VSS	VSS	Y3
D42	VSS	VSS	Y67
D45	VSS		
D49	VSS	VSS_1	CR1
D5	VSS	VSS_2	CR67
D51	VSS	VSS_3	A1
D53	VSS	VSS_4	A67
D57	VSS		
D64	VSS	VSS_DDR_SENSE	A63
D66	VSS	VSS_GPU_SENSE	AE29
D7	VSS	VSS_PCPU_SENSE	BP39
E4	VSS	VSS_SENSE	AY18
E66	VSS		
E67	VSS		

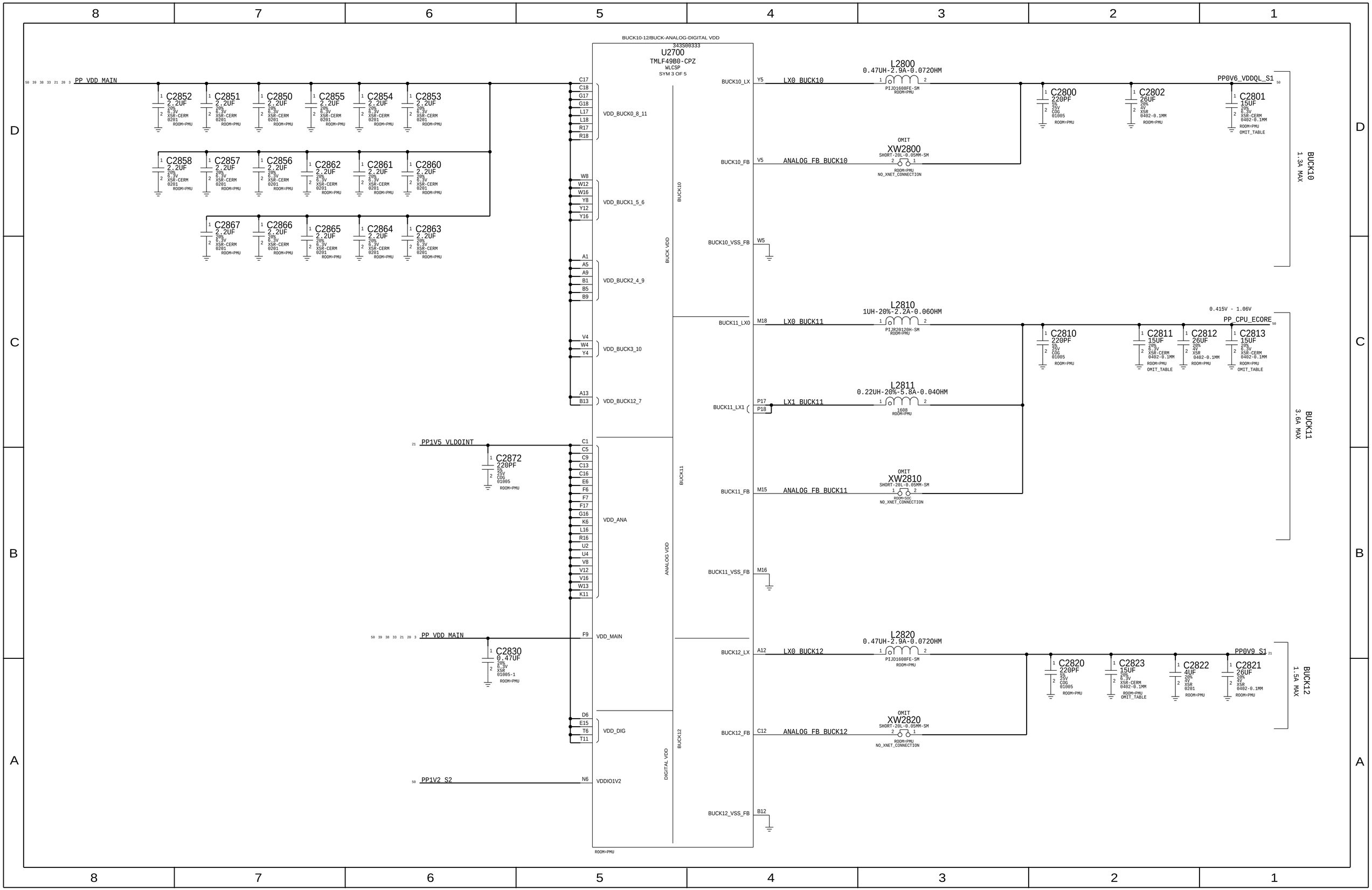
<-- Corner Ball Test Pins. System connects to GND.

ANALOG_VDDQL_DCS_SENSEN OUT 5
ANALOG_GPU_SENSEN OUT 5
ANALOG_CPU_PCORE_SENSEN OUT 5
ANALOG_SOC_SENSE_N OUT 5

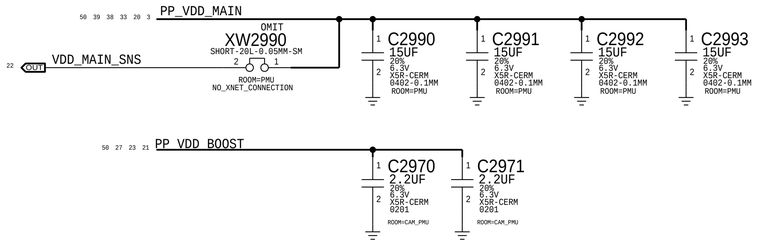
S4E NAND

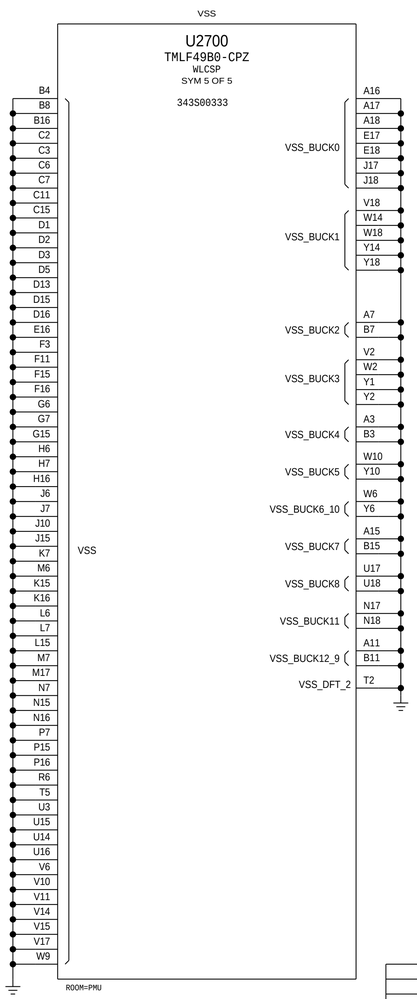

FUTURE COMPATABILITY: R2602 50mohm Max
Default R2602: NO STUFF
196mA MAX
PP1V2_IO_NAND
R2602 0 5% 1/20W MF 0201 ROOM=NAND
NOSTUFF
PP_VDDIO_2_NAND_R
C2630 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=NAND
C2629 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=NAND
C2643 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2645 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2647 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2612 220PF 5% 25V C0G 01005 ROOM=NAND
C2618 100PF 5% 16V NP0-C0G 01005-1 ROOM=NAND
C2614 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2615 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2617 22PF 2% 16V C0G 01005 ROOM=NAND
R2603 0 5% 1/20W MF 0201 ROOM=NAND
267mA MAX S4E (8 dies)
50mA MAX S4E COMPATABILITY MODE
PP1V8_IO
C2641 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2624 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2626 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2610 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
C2611 220PF 5% 25V C0G 01005 ROOM=NAND
1150mA MAX (1us peak power)
PP2V63_NAND
C2613 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=NAND
C2616 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=NAND
C2619 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=NAND
C2621 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=NAND
C2649 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2650 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2651 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2652 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2638 100PF 5% 16V NP0-C0G 01005-1 ROOM=NAND
C2639 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2634 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2635 22PF 2% 16V C0G 01005 ROOM=NAND
C2636 220PF 5% 25V C0G 01005 ROOM=NAND
C2637 100PF 5% 16V NP0-C0G 01005-1 ROOM=NAND
700mA MAX S4E
578mA MAX S4E COMPATABILITY MODE
PP0V9_NAND
C2602 26UF 20% 4V X5R 0402-0.1MM ROOM=NAND
C2605 26UF 20% 4V X5R 0402-0.1MM ROOM=NAND
C2600 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2601 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2622 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2627 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2640 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2642 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2644 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2646 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2603 220PF 5% 25V C0G 01005 ROOM=NAND
C2606 220PF 5% 25V C0G 01005 ROOM=NAND
C2609 100PF 5% 16V NP0-C0G 01005-1 ROOM=NAND
C2607 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2608 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2604 22PF 2% 16V C0G 01005 ROOM=NAND
FUTURE COMPATABILITY
R2625 -> Ferrite Bead (APN: 155S00340)
PP1V8_IO_NAND_F
C2625 4UF 20% 4V X5R 0201 ROOM=NAND
R2625 0.00 5% 1/32W MF 01005 ROOM=NAND
FUTURE COMPATABILITY:
R2663 -> 2 Ohm
PP1V8_IO_NAND_R
R2663 0.00 5% 1/32W MF 01005 ROOM=NAND
C2663 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
FUTURE COMPATABILITY
R2623 -> Ferrite Bead (APN: 155S00340)
PP0V9_NAND_F
R2623 0.00 5% 1/32W MF 01005 ROOM=NAND
PP0V9_NAND
C2623 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
N6 M9 J6 N8 J8 L2 G12 NC J4 NC G6 G8 L6 L8 R6 R8 J2 K9 T5 E2 E10 N2 P9 D3 E12 G4 L12 R2 R4 F3 NC
PCI_AVDD_CLK_1 PCI_AVDD_CLK_2 PCI_AVDD_H PCI_VDD_1 PCI_VDD_2 AVDD18_PLL AN0_VREF AN1_VREF VDD VDDIO_1/GPIO VDDIO_2/NAND VCC VDD_PLL VPP
ROOM=NAND
U2600
NAND-S4E-S5E-MCP-STUDY
LGA
OMIT_TABLE
CLK_AP_TO_NAND_24M M3 CLK_IN
90_PCIE0_AP_TO_NAND_REFCLK_P K11 PCIE_REFCLK_P
90_PCIE0_AP_TO_NAND_REFCLK_N J12 PCIE_REFCLK_M
PCIE0_AP_BI_NAND_CLKREQ_L P5 PCIE_CLKREQ_N
ANALOG_PCIE_NAND_RESREF H7 PCI_RESREF
90_PCIE0_AP_TO_NAND_TX_P M11 PCIE_RX0_P
90_PCIE0_AP_TO_NAND_TX_N N12 PCIE_RX0_M
90_PCIE0_AP_FROM_NAND_RX_P R12 PCIE_TX0_P
90_PCIE0_AP_FROM_NAND_RX_N T11 PCIE_TX0_M
IO_AP_TO_NAND_RESET_L L4 RESET*
TRST* G10
ZQ_C K3
ZQ_N C10
Default C2620: No Stuff
FUTURE COMPATABILITY:
R2604 -> 200 Ohm
C2620 -> 10pF
C2620 10PF 5% 16V NP0/C0G 01005 ROOM=NAND
NOSTUFF
R2604 3.01K 1% 1/32W MF 01005 ROOM=NAND
Board trace <= 0.20hm
ANALOG_NAND_ZQ_C
ANALOG_NAND_ZQ_NEG
R2600 100 0.1% 1/32W MF 01005 ROOM=NAND
R2601 300 0.1% 1/32 MF 01005 ROOM=NAND
FUTURE COMPATABILITY: R2600 -> 300 Ohm
VSS
EXT_D0/BOOT0 B3 GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L
EXT_D1/BOOT1 C4 IO_AP_TO_NAND_FW_STRAP
EXT_D2/BOOT2/SPINAND_SCLK B5 SPI0_AP_TO_S4E_SCLK_BOOT_CONFIG0
EXT_D3/SWD_UID0/SPINAND_MISO C6 SPI0_AP_FROM_S4E_MISO_BOOT_CONFIG2
EXT_D4/UART_RX B7 NC
EXT_D5/SWD_UID1/SPINAND_MOSI C8 SPI0_AP_TO_S4E_MOSI_BOOT_CONFIG1
EXT_D6/UART_TX B9 NC
EXT_D7/SPF B11 IO_PMU_TO_MANY_SYSTEM_ALIVE
EXT_NCE/PERST* E8 PCIE0_AP_TO_NAND_PERST_L
EXT_NRE/JTAG_TMS D7 SWD_AP_BI_NAND_SWDIO
EXT_NWE/JTAG_TCK E6 SWD_NUB_TO_MANY_SWCLK
EXT_RNB/JTAG_TDO E4
EXT_CLE/JTAG_TDI D5 NC
EXT_ALE/JTAG_SEL D9
DROOP_N T3
WP_N G2 PP_VDDIO_2_NAND_R
FUTURE COMPATABILITY

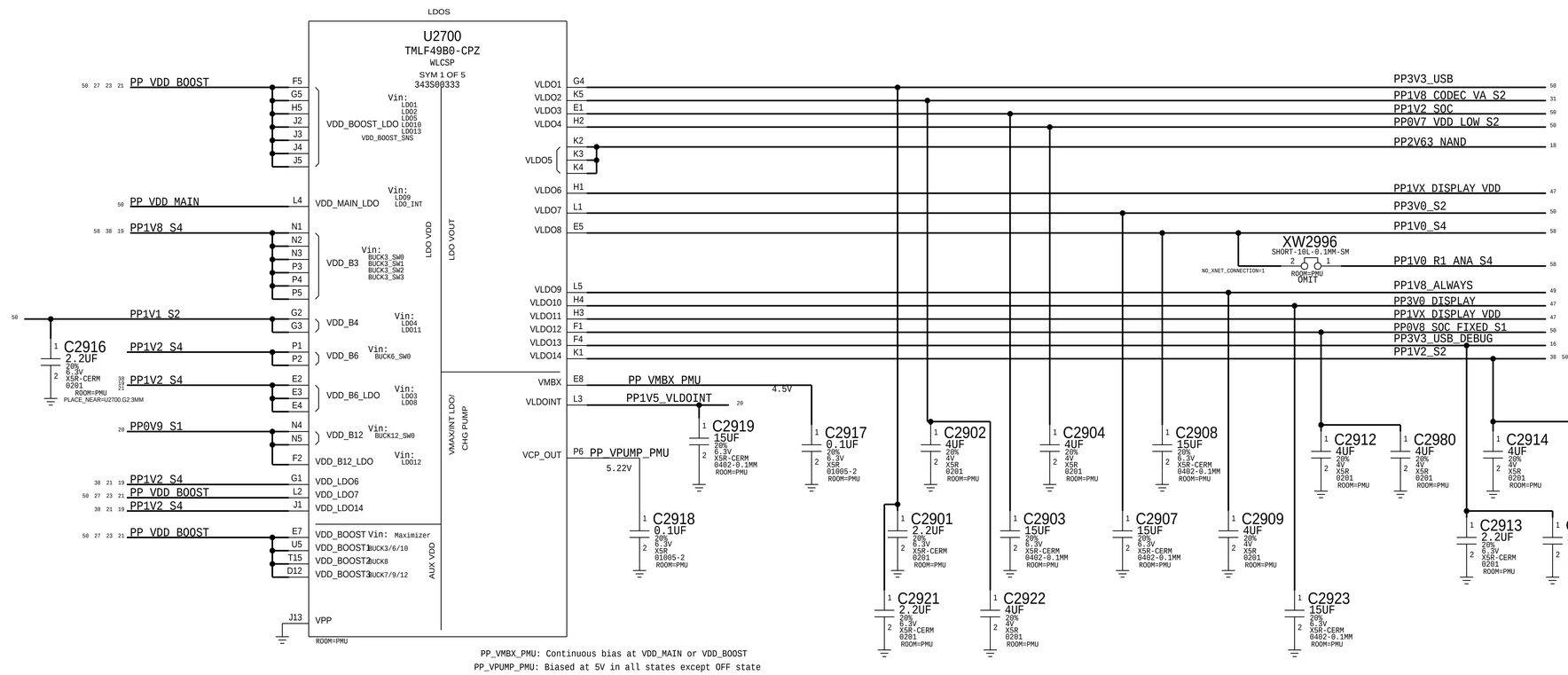

BUCK0-9/SWITCHES
343S00333
U2700
TMLF49B0-CPZ
WLCSP
SYM 2 OF 5
BUCK4
2.7A MAX
V_BUCK4_Default = 1.0625V
PP1V1_S2
C2744 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2743 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2742 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2741 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2740 220PF 5% 25V COG 01005 ROOM=PMU
L2740 1.0UH-20%-1.55A-0.063OHM PIJD2012-SM ROOM=PMU
L2741 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU
OMIT XW2740 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
LX0 BUCK4 A4 BUCK4_LX0
LX1 BUCK4 A2 B2 BUCK4_LX1
ANALOG_FB_BUCK4 D4 C4 BUCK4_FB BUCK4_VSS_FB
BUCK5
3.2A MAX
PP_AVE_S1
C2753 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU OMIT_TABLE
C2752 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU OMIT_TABLE
C2751 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU OMIT_TABLE
C2750 220PF 5% 25V COG 01005 ROOM=PMU
L2750 1.0UH-20%-1.55A-0.063OHM PIJD2012-SM ROOM=PMU
L2751 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU
OMIT XW2750 SHORT-10L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION
LX0 BUCK5 Y9 BUCK5_LX0
LX1 BUCK5 W11 Y11 BUCK5_LX1
ANALOG_FB_BUCK5 U9 V9 BUCK5_FB BUCK5_VSS_FB
BUCK6
1.5A MAX
V_BUCK6_Default = 1.240625V
PP1V2_S4
C2762 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2761 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2763 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU
C2760 220PF 5% 25V COG 01005 ROOM=PMU
L2760 0.47UH-3.7A-0.0340HM PIJD16140H-SM ROOM=PMU
OMIT XW2760 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
LX0 BUCK6 Y7 BUCK6_LX
ANALOG_FB_BUCK6 V7 W7 BUCK6_FB BUCK6_VSS_FB
BUCK7
2.2A MAX
0.735V - 1.01V
PP_SRAM_S1
C2772 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU
C2771 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2770 220PF 5% 25V COG 01005 ROOM=PMU
L2770 0.47UH-20%-4.0A-0.050HM PIJD2012-SM ROOM=PMU
OMIT XW2770 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
LX0 BUCK7 A14 B14 BUCK7_LX
ANALOG_FB_BUCK7 D14 C14 BUCK7_FB BUCK7_VSS_FB
BUCK8
1.5A MAX
0.675V - 1.06V
PP_DISP_S1
C2781 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2782 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU
C2780 220PF 5% 25V COG 01005 ROOM=PMU
L2780 0.47UH-2.9A-0.0720HM PIJD1608FE-SM ROOM=PMU
OMIT XW2780 SHORT-10L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION
LX0 BUCK8 T18 BUCK8_LX
ANALOG_FB_BUCK8 T16 T17 BUCK8_FB BUCK8_VSS_FB
BUCK9
1.3A MAX
0.600V - 0.875V
PP_DCS_S1
C2791 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2792 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2790 220PF 5% 25V COG 01005 ROOM=PMU
L2790 0.47UH-2.9A-0.0720HM PIJD1608FE-SM ROOM=PMU
OMIT XW2790 SHORT-10L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
LX0 BUCK9 A10 BUCK9_LX
ANALOG_FB_BUCK9 C10 B10 BUCK9_FB BUCK9_VSS_FB
ROOM=PMU
BUCK0
15.2A MAX
BUCK0_LX0 F18
L2700 1UH-20%-3.6A-0.0620HM PIWE20160H-SM ROOM=PMU
LX0 BUCK0
C2700 220PF 5% 25V COG 01005 ROOM=PMU
C2701 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU
C2702 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU
0.4V - 1.15V
PP_CPU_PCORE
BUCK0_LX1 B17 B18
L2701 0.1UH-20%-6.1A-0.019OHM MTFE2016-2SM
LX1 BUCK0 UPPER_COIL_IN UPPER_COIL_OUT
BUCK0_LX3 D17 D18
LX3 BUCK0 LOWER_COIL_IN LOWER_COIL_OUT
BUCK0_LX2 H17 H18
L2702 0.1UH-20%-6.1A-0.019OHM MTFE2016-2SM
LX2 BUCK0 UPPER_COIL_IN UPPER_COIL_OUT
BUCK0_LX4 K17 K18
LX4 BUCK0 LOWER_COIL_IN LOWER_COIL_OUT
BUCK0_FB H15 ANALOG_FB_BUCK0
R2700 0.00 0% MF 1/32W 01005 ROOM=SOC NO_XNET_CONNECTION
ANALOG_FB_BUCK0_R
XW2700 SHORT-10L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION
BUCK0_VSS_FB J16
BUCK1
10A MAX
BUCK1_LX0 Y13
L2710 1UH-20%-3.6A-0.0620HM PIWE20160H-SM ROOM=PMU
LX0 BUCK1
C2710 220PF 5% 25V COG 01005 ROOM=PMU
C2711 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU OMIT_TABLE
C2712 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU OMIT_TABLE
0.4V - 1.06V
1.03V for overdrive only
PP_GPU
BUCK1_LX1 W17 Y17
L2711 0.1UH-20%-6.1A-0.019OHM MTFE2016-2SM
LX1 BUCK1 UPPER_COIL_IN UPPER_COIL_OUT
BUCK1_LX2 W15 Y15
LX2 BUCK1 LOWER_COIL_IN LOWER_COIL_OUT
BUCK1_FB U13
ANALOG_FB_BUCK1
OMIT XW2710 SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION
BUCK1_VSS_FB V13
BUCK2
4.9A MAX
BUCK2_LX0 A8
L2720 1UH-20%-2.2A-0.060HM PIJR20120H-SM ROOM=PMU
LX0 BUCK2
C2720 220PF 5% 25V COG 01005 ROOM=PMU
C2721 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU OMIT_TABLE
C2722 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU OMIT_TABLE
C2723 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU OMIT_TABLE
0.67V/0.80V
PP_SOC_S1
BUCK2_LX1 A6 B6
L2721 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU
LX1 BUCK2
BUCK2_FB D8
ANALOG_FB_BUCK2
OMIT XW2720 SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION
BUCK2_VSS_FB C8
BUCK3
2A MAX
BUCK3_LX V3 W3 Y3
L2730 1UH-20%-3.6A-0.0620HM PIWE20160H-SM ROOM=PMU
LX0 BUCK3
C2730 220PF 5% 25V COG 01005 ROOM=PMU
C2731 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU OMIT_TABLE
C2732 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2733 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
C2734 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU OMIT_TABLE
PP1V8_S4
BUCK3_FB W1
ANALOG_FB_BUCK3
XW2730 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
OMIT
BUCK3_VSS_FB V1
BUCK SWITCHES
BUCK_SWI0 R3 R4 BUCK3_SW0 PP1V8_S2
BUCK_SWI1 M2 M3 BUCK3_SW1 PP1V8_IO
BUCK_SWI2 R5 BUCK3_SW2 PP1V8_TOUCH_S2
BUCK_SWI3 M1 BUCK3_SW3 PP1V8_NFC_S2
BUCK_SWI4 R1 R2 BUCK6_SW0 PP1V2_IO_NAND
BUCK_SWI5 M4 M5 BUCK12_SW0 PP0V9_NAND


BUCK10-12/BUCK-ANALOG-DIGITAL VDD
343S00333
U2700
TMLF49B0-CPZ
WLCSP
SYM 3 OF 5
PP VDD MAIN
C2852 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2851 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2850 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2855 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2854 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2853 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2858 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2857 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2856 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2862 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2861 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2860 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2867 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2866 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2865 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2864 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2863 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C17 C18 G17 G18 L17 L18 R17 R18
VDD_BUCK0_8_11
W8 W12 W16 Y8 Y12 Y16
VDD_BUCK1_5_6
A1 A5 A9 B1 B5 B9
VDD_BUCK2_4_9
V4 W4 Y4
VDD_BUCK3_10
A13 B13
VDD_BUCK12_7
PP1V5 VLDOINT
C2872 220PF 5% 25V C0G 01005 ROOM=PMU
C1 C5 C9 C13 C16 E6 F6 F7 F17 G16 K6 L16 R16 U2 U4 V8 V12 V16 W13 K11
VDD_ANA
PP VDD MAIN
C2830 0.47UF 20% 6.3V X5R 01005-1 ROOM=PMU
F9
VDD_MAIN
D6 E15 T6 T11
VDD_DIG
PP1V2 S2
N6
VDDIO1V2
BUCK VDD
BUCK10
ANALOG VDD
BUCK11
DIGITAL VDD
BUCK12
ROOM=PMU
BUCK10_LX
Y5
LX0 BUCK10
L2800
0.47UH-2.9A-0.0720HM
PIJD1608FE-SM
ROOM=PMU
C2800 220PF 5% 25V C0G 01005 ROOM=PMU
C2802 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
PP0V6_VDDQL_S1
C2801 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU OMIT_TABLE
BUCK10_FB
V5
ANALOG FB BUCK10
OMIT
XW2800
SHORT-20L-0.05MM-SM
ROOM=PMU NO_XNET_CONNECTION
BUCK10 1.3A MAX
BUCK10_VSS_FB
W5
BUCK11_LX0
M18
LX0 BUCK11
L2810
1UH-20%-2.2A-0.060HM
PIJR20120H-SM
ROOM=PMU
C2810 220PF 5% 25V C0G 01005 ROOM=PMU
C2811 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU OMIT_TABLE
C2812 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
0.415V - 1.06V
PP_CPU_ECORE
C2813 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU OMIT_TABLE
BUCK11_LX1
P17 P18
LX1 BUCK11
L2811
0.22UH-20%-5.8A-0.040HM
1608
ROOM=PMU
BUCK11_FB
M15
ANALOG FB BUCK11
OMIT
XW2810
SHORT-20L-0.05MM-SM
ROOM=SOC NO_XNET_CONNECTION
BUCK11 3.6A MAX
BUCK11_VSS_FB
M16
BUCK12_LX
A12
LX0 BUCK12
L2820
0.47UH-2.9A-0.0720HM
PIJD1608FE-SM
ROOM=PMU
C2820 220PF 5% 25V C0G 01005 ROOM=PMU
C2823 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=PMU OMIT_TABLE
C2822 4UF 20% 4V X5R 0201 ROOM=PMU
PP0V9_S1
C2821 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU
BUCK12_FB
C12
ANALOG FB BUCK12
OMIT
XW2820
SHORT-20L-0.05MM-SM
ROOM=PMU NO_XNET_CONNECTION
BUCK12 1.5A MAX
BUCK12_VSS_FB
B12

PMU - LDOs







PP_VMBX_PMU: Continuous bias at VDD_MAIN or VDD_BOOST
PP_VPUMP_PMU: Biased at 5V in all states except OFF state

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_100UM	P	PWR_100UM	PP1V5_VLDOINT	?
PWR_DEFAULT	P	PWR_DEFAULT	PP_VMBX_PMU,PP_VPUMP_PMU	?

PMU - GPIOs

CONTROL PIN NOTES:

NOTE (1):INPUT PULL-DOWN 100-300k
NOTE (2):INPUT PULL-DOWN 1M
NOTE (3):INPUT PULL-UP OR DOWN 100k-300k
NOTE (4):OUTPUT OPEN-DRAIN, REQUIRES PULL-UP

AMUX CAPS

AMUX_PMU_FROM_CAM_PMU 22 25 — C3071 1000PF 10% 10V X5R 01005 ROOM=PMU
AMUX_PMU_FROM_GECKO 22 34 — C3072 1000PF 10% 10V X5R 01005 ROOM=PMU
AMUX_RCAM_PVDD 22 26 — C3073 1000PF 10% 10V X5R 01005 ROOM=PMU

COLD_RESET & SYSTEM_ALIVE

PP1V8_S2 46 50
R3061 100K 5% 1/32W MF 01005 ROOM=PMU
R3062 100K 5% 1/32W MF 01005 ROOM=PMU
IO_PMU_TO_MANY_SYSTEM_ALIVE 18 22
IO_PMU_TO_SYSTEM_RESET_L 13 22 38

Only has DS control when powered by VBUCK3

Amux pins A1, A6 and A7 are used for ADC offset cal
Do not change without contacting FCT team

NTCs

FOREHEAD NTC

C3041 100PF 5% 16V NP0-C0G 01005-1 ROOM=PMU
R3041 10KOHM-1% 01005 ROOM=PMU
NTC_FOREHEAD_P 22
NTC_FOREHEAD_N
OMIT XW3041 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

RADIO BB NTC ON MLB_BOT

38 NTC_RADIO_BB_N
OMIT XW3042 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

RADIO PA NTC ON RADIOS PAGE

AP NTC

C3044 100PF 5% 16V NP0-C0G 01005-1 ROOM=PMU
R3044 10KOHM-1% 01005 ROOM=PMU
NTC_AP_P 22
NTC_AP_N
OMIT XW3044 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

BATTERY NTC

C3045 100PF 5% 16V NP0-C0G 01005-1 ROOM=PMU
R3045 10KOHM-1% 01005 ROOM=PMU
NTC_BATTERY_P 22
NTC_BATTERY_N
OMIT XW3045 SHORT-20L-0.05MM-SM ROOM=PMU

U2700 TMLF49B0-CPZ WLCSP SYM 4 OF 5 (SYSTEM INTERFACE/AUX 343S00333)

Signal	Pin	Net	Dir / Notes
RESET_IN1	L12	IO_AP_TO_PMU_RESET	13 5 IN
RESET_IN2	M12	IO_HYDRA_TO_PMU_RESET	36 IN
RESET_IN3	K13	IO_AP_TO_PMU_SOCHOT_L	7 5 IN
RESET*	L10	IO_PMU_TO_SYSTEM_RESET_L	38 22 13 OUT
SHDN	N11	NC	
ACTIVE_READY	K10	IO_PMU_TO_AP_HYDRA_ACTIVE_READY	36 7 5 OUT
SLEEP_32K	R7	CLK_PMU_TO_AOP_32K	13 5 OUT
OUT_32K	P8	CLK_PMU_TO_TOUCH_32K	48 OUT
SYS_ALIVE	L11	IO_PMU_TO_MANY_SYSTEM_ALIVE	22 18 OUT
FORCE_SYNC	P13	GPIO_TOUCH_TO_MANY_SCAN_ACTIVE	49 48 38 25 23 IN
DBLCLICK_DET	N14	GPIO_PMU_TO_AP_DOUBLE_CLICK_DET_L	11 OUT
CRASH*	M11	NC	
FAULT_OUT*	K12	IO_PMU_TO_DOTARA_RESET_L	49 33 OUT
LDO13_EN	M9	IO_HYDRA_TO_NUB_PMU_DOCK_CONNECT	36 13 IN
SPMI_SCLK	M8	SPMI0_NUB_TO_PMU_DOTARA_CLK	49 13 IN
SPMI_SDATA	N8	SPMI0_NUB_BI_PMU_DOTARA_DATA	49 13 BI
AMUX_A<0>	G13	AMUX_PMU_FROM_AP_ANALOGMUX_OUT	7 IN
AMUX_A<1>	E13	CKPLUS_NATIVE=SINGLE_COMP_NET	
AMUX_A<2>	F13	AMUX_PMU_TO_ADC_IN	22
AMUX_A<3>	E12	AMUX_PMU_FROM_GECKO	34 22 IN
AMUX_A<4>	E14	AMUX_RCAM_PVDD	26 22 IN
AMUX_A<5>	F14	IO_HYDRA_TO_PMU_USB_BRICK_ID_TIA	36 30 22 IN
AMUX_A<6>	G14		
AMUX_A<7>	H14		
AMUX_AY	E11	AMUX_PMU_AY	38 OUT
AMUX_B<0>	F12	GPIO_AP_TO_AMUX_PMU_SYNC	56 IN
AMUX_B<1>	D10	ANALOG_BMU_DIFF_AMP_ISENSE	39 IN
AMUX_B<2>	G8	AMUX_PMU_FROM_DISPLAY	47 IN
AMUX_B<3>	G9	AMUX_PMU_FROM_CAM_PMU	25 22 IN
AMUX_B<4>	G10	GPIO_CAM_PMU1_FROM_RIGEL_INT	28 25 5 IN
AMUX_B<5>	H8	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	56 IN
AMUX_B<6>	H9	CLK_AP_TO_PMU_TST_CLKOUT	7 5 IN
AMUX_B<7>	H10	CLK_GPIO_PMU_TO_WLAN_R1_32K	58 56 38 IN
AMUX_BY	D11	AMUX_PMU_BY	38 36 OUT
TDEV1	H12	NTC_FOREHEAD_P	22
TDEV2	H13	NTC_RADIO_BB_P	38 IN
TDEV3	J14	NTC_RADIO_PA_P	58
TDEV4	G12	NTC_AP_P	22
TDEV5	H11	NTC_BATTERY_P	22
TCAL	G11	ANALOG_PMU_TCAL	
XIN	T1	CLK_PMU_XTAL1_32K	
XOUT	U1	CLK_PMU_XTAL2_32K	
VSS	T4	VSS_PMU_RTC	22
NXTAL_MEMS	T3		
DFT_CTRL<0>	L9		
DFT_CTRL<1>	N9	SWD_NUB_TO_MANY_SWCLK	58 38 18 13 IN

ROOM=PMU

Signal	Pin	Net	Dir / Notes
IREF	F8	ANALOG_PMU_IREF	
VREF	E9	ANALOG_PMU_VREF	
VSS_REF	D9	ANALOG_PMU_VSS_REF	
VREF_ADC	J12	ANALOG_PMU_VREF_ADC	
VDD_MAIN_SNS	D7	VDD_MAIN_SNS	
UVWARN*	N10	IO_PMU_TO_AP_PRE_UVLO_L	IN 21 / OUT 5 7
VDD_BOOST_UVLO_L	U6	NC	
CPU_TRIGGER0*	P14	IO_AP_FROM_PMU_COMP_CPU_TRIGGER0_L	OUT 7 33
CPU_TRIGGER1*	R15	IO_AP_FROM_PMU_CPU_TRIGGER1_L	OUT 7
GPU_TRIGGER0*	R14	IO_AP_FROM_PMU_GPU_TRIGGER0_L	OUT 7
GPU_TRIGGER1*	T14	IO_AP_FROM_PMU_GPU_TRIGGER1_L	OUT 7
BRICK_ID1	J8	IO_HYDRA_TO_PMU_USB_BRICK_ID_TIA	IN 22 30 36
BRICK_ID2	J9	ANALOG_PMU_VDD_MAIN_SENSE_FILT	22
ADC_IN	J11	AMUX_PMU_TO_ADC_IN	22
IBAT	F10	ANALOG_PMU_VDD_MAIN_ISENSE	IN 39
VBAT	E10	ANALOG_PMU_VDD_MAIN_VSENSE_2	IN 39
BUTTON1	M14	IO_BUTTON_VOL_DOWN_L	IN 49
BUTTON2	M13	IO_BUTTON_SIDE_L	IN 44
BUTTON3	L13	IO_BUTTON_VOL_UP_L	IN 49
BUTTON4	K14	IO_BUTTON_RINGER_A	IN 49
BUTTONO1	L14	IO_PMU_TO_AP_VOL_DOWN_L	OUT 7
BUTTONO2	N13	IO_PMU_TO_AP_SIDE_L	OUT 7
BUTTONO3	N12	NC	
GPIO1	L8	GPIO_PMU_TO_CCG2_RESET_L	56
GPIO2	R13	NC_PMU_GPIO_2	56
GPIO3	T13	SWD_NUB_BI_PMU_SWDIO	56
GPIO4	T12	GPIO_PMU_FROM_WLAN_HOST_WAKE	56
GPIO5	R12	GPIO_PMU_NFC_TO_ARC_TRIG	56
GPIO6	P12	GPIO_PMU_NFC_TO_ARC_RESET_L	56
GPIO7	U12	NC_PMU_GPIO_7	56
GPIO8	U11	NC_PMU_GPIO_8	56
GPIO9	R11	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L	56
GPIO10	U10	NC_PMU_GPIO_10	56
GPIO11	P11	GPIO_PMU_FROM_CHARGER_INT_L	56
GPIO12	T10	GPIO_PMU_FROM_CODEC_WAKE_L	56
GPIO13	P10	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	56
GPIO14	R10	GPIO_PMU_TO_R1_RESET_L	56
GPIO15	K9	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	56
GPIO16	M10	CLK_GPIO_PMU_TO_DISPLAY_32K	56
GPIO17	T9	GPIO_PMU_TO_WLAN_REG_ON	56
GPIO18	R9	CLK_GPIO_PMU_TO_WLAN_R1_32K	56
GPIO19	U8	GPIO_PMU_TO_SPKAMP_BOT_RESET_L	56
GPIO20	P9	GPIO_PMU_TO_DOTARA_EN_EXT_1V8	56
GPIO21	T8	GPIO_PMU_TO_BBPMU_RESET_L	56
GPIO22	R8	GPIO_PMU_TO_NFC_EN	56
GPIO23	U7	GPIO_PMU_TO_BOOST_EN	56
GPIO24	T7	GPIO_PMU_TO_DISPLAY_PANICB	56
GPIO25	K8	GPIO_PMU_TO_DISPLAY_RESET_L	56

R3010 200K 1% 1/32W MF 01005 ROOM=PMU
C3010 1.5UF 20% 6.3V CER-X5R 0201
OMIT XW3046 SHORT-20L-0.05MM-SM ROOM=PMU
C2899 0.1UF 20% 6.3V X5R 01005-2 ROOM=PMU
R3090 200K 1% 1/32W MF 01005 ROOM=PMU — REQUIRED TO PREVENT STARTUP GLITCH
R3091 200K 1% 1/32W MF 01005 ROOM=PMU NOSTUFF

PULL-DOWN REQUIRED TO PREVENT STARTUP GLITCH
R3091: NOSTUFF
R8010: 100K Pull-down

R3011 200K 1% 1/32W MF 01005 ROOM=PMU NOSTUFF

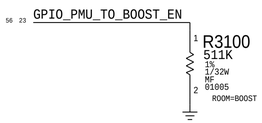
C3020 100PF 5% 16V NP0-C0G 01005-1 ROOM=PMU
R3020 3.92K 0.1% 1/32W TK 01005 ROOM=PMU

Y3000 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM CRITICAL ROOM=PMU
C3051 22PF 5% 16V C0G 01005 ROOM=PMU CRITICAL
C3052 22PF 5% 16V C0G 01005 ROOM=PMU CRITICAL
VSS_PMU_RTC 22
OMIT XW3000 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

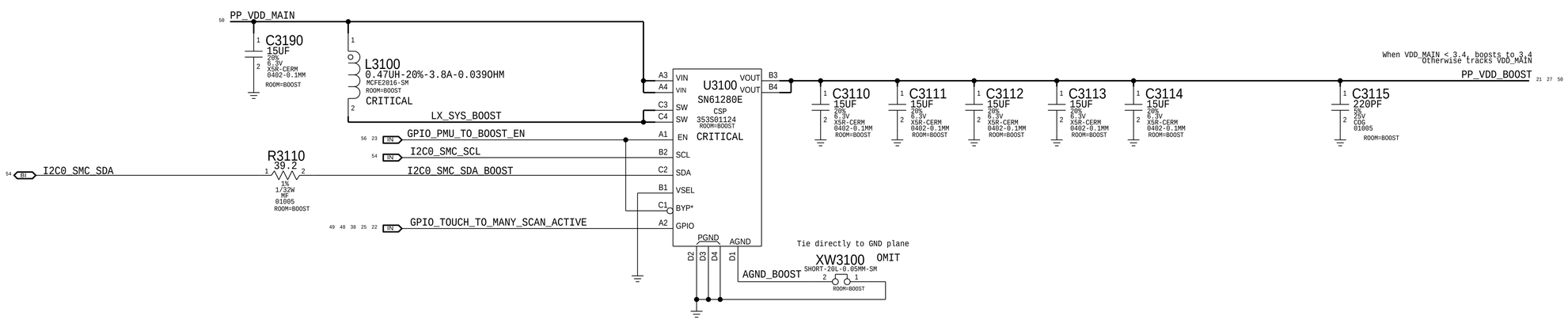
PMU_VDD_RTC_DIG cap tracker rdar#: 29938782

CRITICAL
R3003 9.53K 1% 1/32W MF 01005 ROOM=PMU
39 ANALOG_PMU_VDD_MAIN_SENSE — ANALOG_PMU_VDD_MAIN_SENSE_FILT 22
C3003 0.1UF 20% 6.3V X5R 01005-2 ROOM=PMU

Boost Enable Pull



BOOST

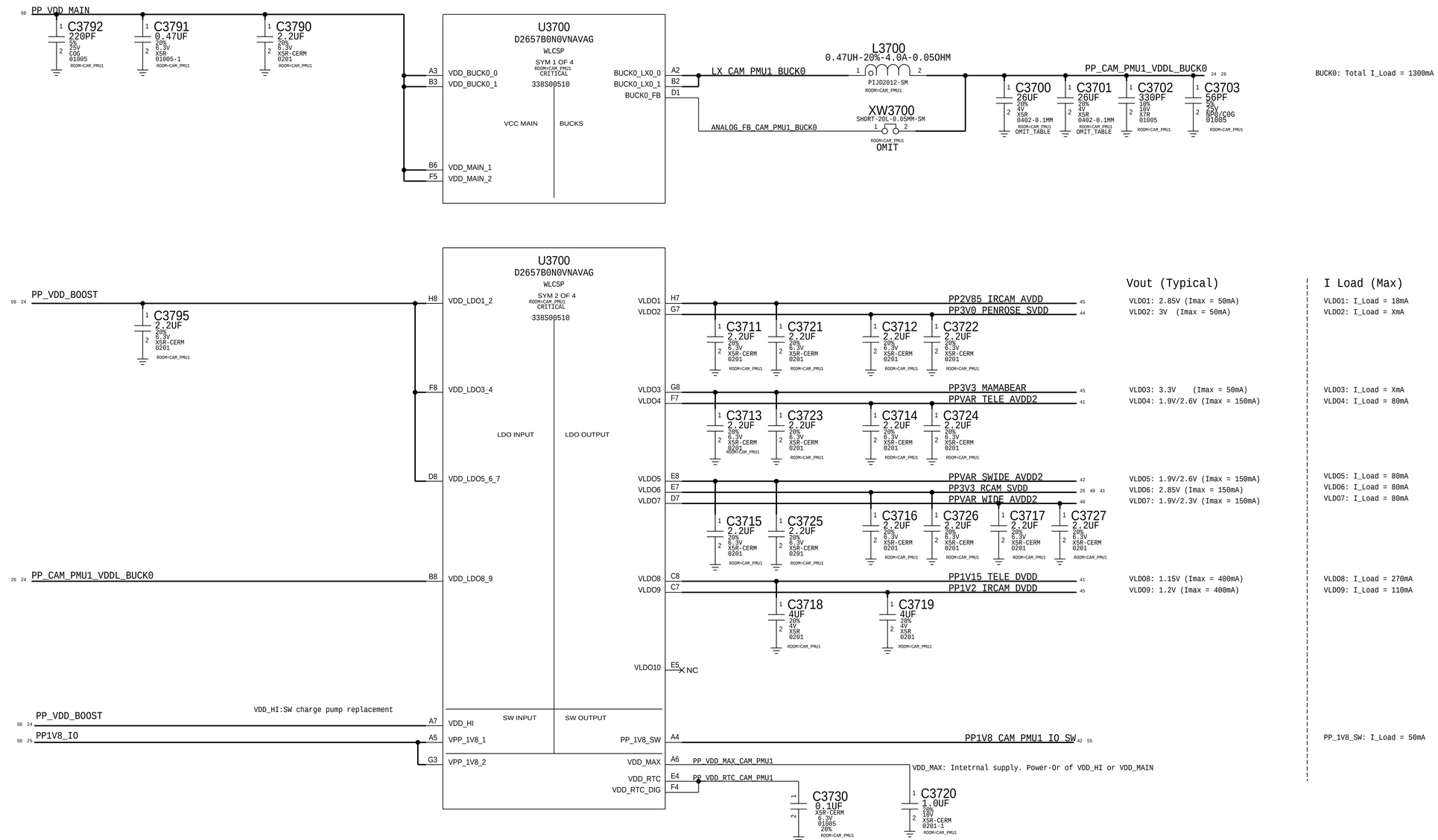


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00871	152S00869	ALT_PARTS	ALL	IND,PWR,0.47UH,20%,4A,50MOHM,TA2YO,2016
152S00873	152S00869	ALT_PARTS	ALL	IND,PWR,0.47UH,20%,3.6A,55MOHM,TDK,2016

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	CONN TYP	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_SHAPE	P	PWR_SHAPE	LX_SYS_BOOST	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	CONN TYP	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
SWITCHING	S	A_DIELECTRIC_1.5X	LX_SYS_BOOST	?

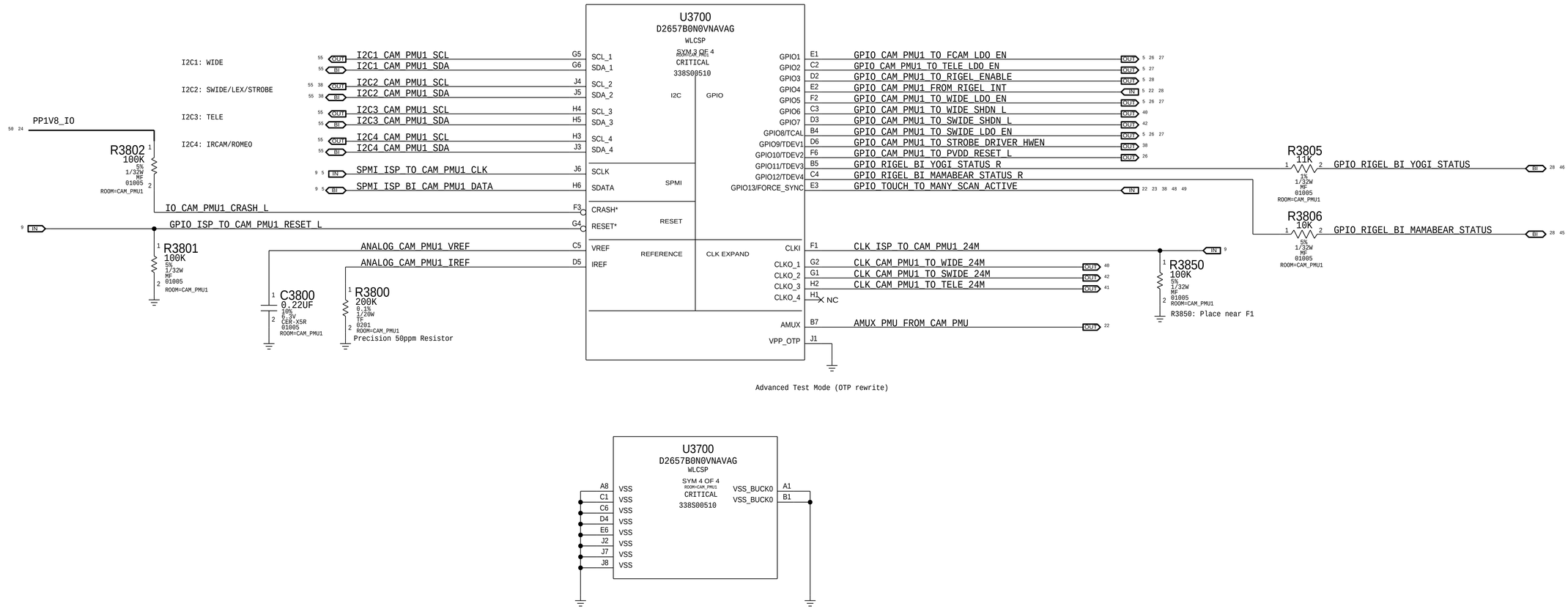
CAMERA PMU1



CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHANGE
CLASS NAME	*****	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_50UM	P	PWR_50UM	PP_VDD_MAX_CAM_PMU1,PP_VDD_RTC_CAM_PMU1	?
PWR_80UM	P	PWR_80UM	PP1V8_IRCAM_VDD10*,PP3V3_MAMABEAR*	?
PWR_100UM	P	PWR_100UM	PP1V8_CAM_PMU1_IO_SW	?
PWR_100UM	P	PWR_100UM	PP2V85_IRCAM_AVDD	?
PWR_200UM	P	PWR_200UM	PPVAR_WIDE_AVDD2,PPVAR_SWIDE_AVDD2	?
PWR_200UM	P	PWR_200UM	PP1V2_FCAM_DVDD	?
PWR_SHAPE	P	PWR_SHAPE	LX_CAM_PMU1_*,PP_CAM_PMU1_VDDL_BUCK0	?
PWR_SHAPE	P	PWR_SHAPE	PP1V2_IRCAM_DVDD	?
PWR_SHAPE	P	PWR_SHAPE	PP1V15_TELE_DVDD	?

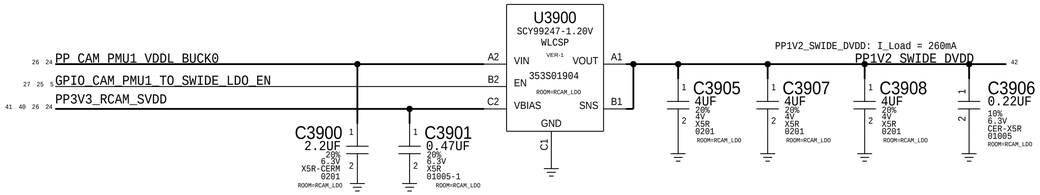
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHANGE
CLASS NAME	*****	CONSTRAIN SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_100UM	S	100UM-249UM_SPACING	PP1V8_CAM_PMU1_IO_SW	?
S_PWR_100UM	S	100UM-249UM_SPACING	PP2V85_IRCAM_AVDD*	?
S_PWR_200UM	S	100UM-249UM_SPACING	PPVAR_WIDE_AVDD2,PPVAR_SWIDE_AVDD2	?
S_PWR_200UM	S	100UM-249UM_SPACING	PP1V2_FCAM_DVDD	?
S_PWR_SHAPE	S	250UM+_SPACING	PP_CAM_PMU1_VDDL_BUCK0	?
S_PWR_SHAPE	S	250UM+_SPACING	PP1V2_IRCAM_DVDD	?
S_PWR_SHAPE	S	250UM+_SPACING	PP1V15_TELE_DVDD	?
SWITCHING	S	A_DIELECTRIC_1.5X	LX_CAM_PMU1_*	?

CAMERA PMU1


U3700
D2657B0N0VNAVAG
WLCSP
SYM 3 OF 4
ROOM=CAM_PMU1
CRITICAL
338S00510
I2C
GPIO
SPMI
RESET
REFERENCE
CLK EXPAND
I2C1: WIDE
I2C2: SWIDE/LEX/STROBE
I2C3: TELE
I2C4: IRCAM/ROMEO
I2C1 CAM PMU1 SCL
I2C1 CAM PMU1 SDA
I2C2 CAM PMU1 SCL
I2C2 CAM PMU1 SDA
I2C3 CAM PMU1 SCL
I2C3 CAM PMU1 SDA
I2C4 CAM PMU1 SCL
I2C4 CAM PMU1 SDA
SPMI ISP TO CAM PMU1 CLK
SPMI ISP BI CAM PMU1 DATA
PP1V8_IO
R3802
100K
5%
1/32W
MF
01005
ROOM=CAM_PMU1
IO CAM PMU1 CRASH L
GPIO ISP TO CAM PMU1 RESET L
R3801
100K
5%
1/32W
MF
01005
ROOM=CAM_PMU1
ANALOG CAM PMU1 VREF
ANALOG CAM PMU1 IREF
C3800
0.22UF
10%
6.3V
CER-X5R
01005
ROOM=CAM_PMU1
R3800
200K
0.1%
1/20W
TF
0201
ROOM=CAM_PMU1
Precision 50ppm Resistor
GPIO CAM PMU1 TO FCAM LDO EN
GPIO CAM PMU1 TO TELE LDO EN
GPIO CAM PMU1 TO RIGEL ENABLE
GPIO CAM PMU1 FROM RIGEL INT
GPIO CAM PMU1 TO WIDE LDO EN
GPIO CAM PMU1 TO WIDE SHDN L
GPIO CAM PMU1 TO SWIDE SHDN L
GPIO CAM PMU1 TO SWIDE LDO EN
GPIO CAM PMU1 TO STROBE DRIVER HWEN
GPIO CAM PMU1 TO PVDD RESET L
GPIO RIGEL BI YOGI STATUS R
GPIO TOUCH TO MANY SCAN ACTIVE
R3805
11K
1%
1/32W
MF
01005
ROOM=CAM_PMU1
GPIO RIGEL BI YOGI STATUS
R3806
10K
5%
1/32W
MF
01005
ROOM=CAM_PMU1
GPIO RIGEL BI MAMABEAR STATUS
CLK ISP TO CAM PMU1 24M
CLK CAM PMU1 TO WIDE 24M
CLK CAM PMU1 TO SWIDE 24M
CLK CAM PMU1 TO TELE 24M
R3850
100K
5%
1/32W
MF
01005
ROOM=CAM_PMU1
R3850: Place near F1
AMUX PMU FROM CAM PMU
Advanced Test Mode (OTP rewrite)

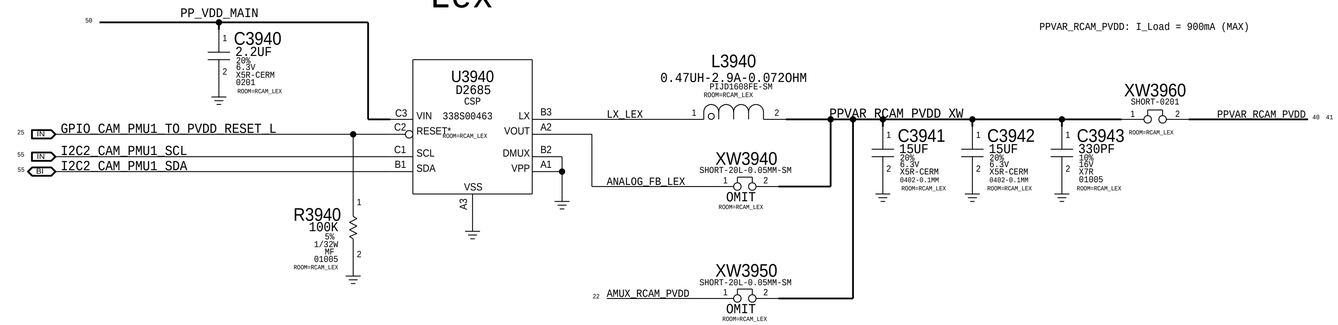
U3700
D2657B0N0VNAVAG
WLCSP
SYM 4 OF 4
ROOM=CAM_PMU1
CRITICAL
338S00510
VSS
VSS_BUCK0

SWIDE VDDL LDO

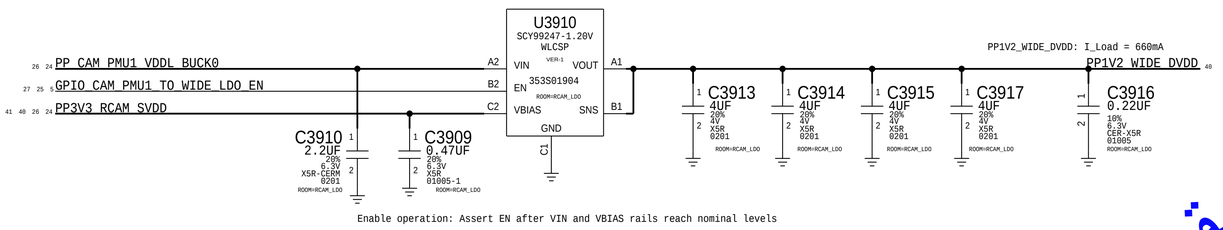


Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

Lex

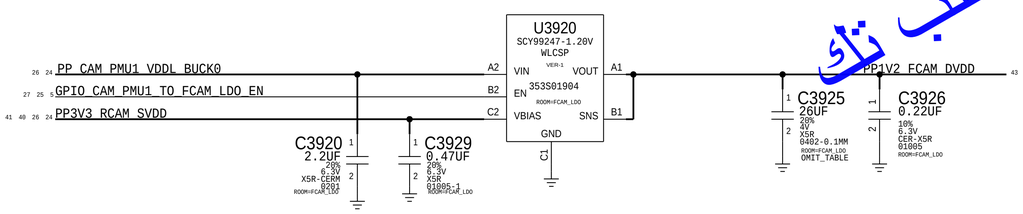


Wide VDDL LDO



Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

FCAM VDDL LDO



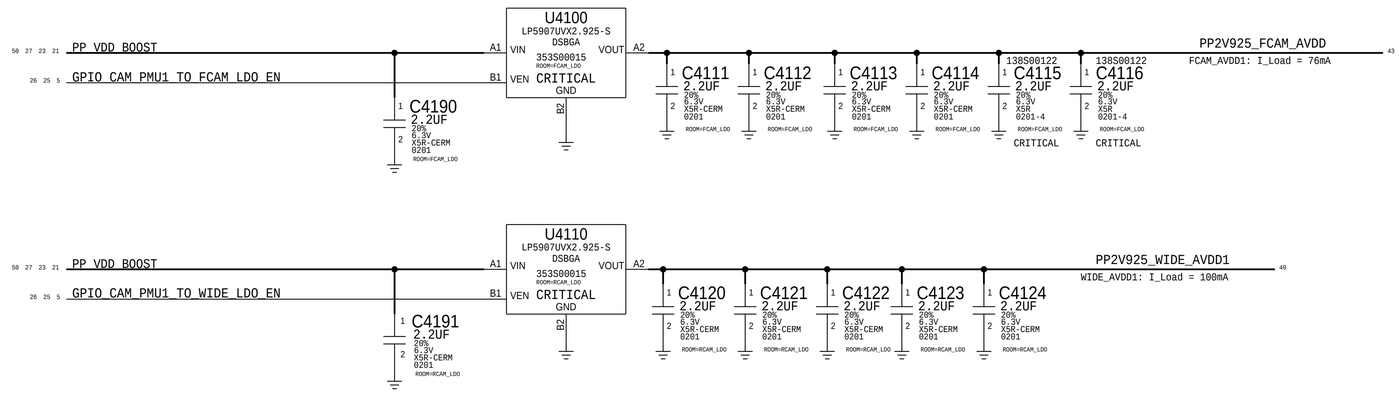
Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

علي البحر -فريق الهارد حلب تك

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_SHAPE	P	PWR_SHAPE	PPVAR_RCAM_PVDD,PPVAR_RCAM_PVDD_XW	?
PWR_SHAPE	P	PWR_SHAPE	PP1V2_WIDE_DVDD,PP1V2_SWIDE_DVDD	?
PWR_SHAPE	P	PWR_SHAPE	LX_LEX	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_SHAPE	S	250UM+_SPACING	PPVAR_RCAM_PVDD,PPVAR_RCAM_PVDD_XW	?
S_PWR_SHAPE	S	250UM+_SPACING	PP1V2_WIDE_DVDD,PP1V2_SWIDE_DVDD	?
SWITCHING	S	A_DIELECTRIC_1.5X	LX_LEX	?

CAMERA VDDH LDOs

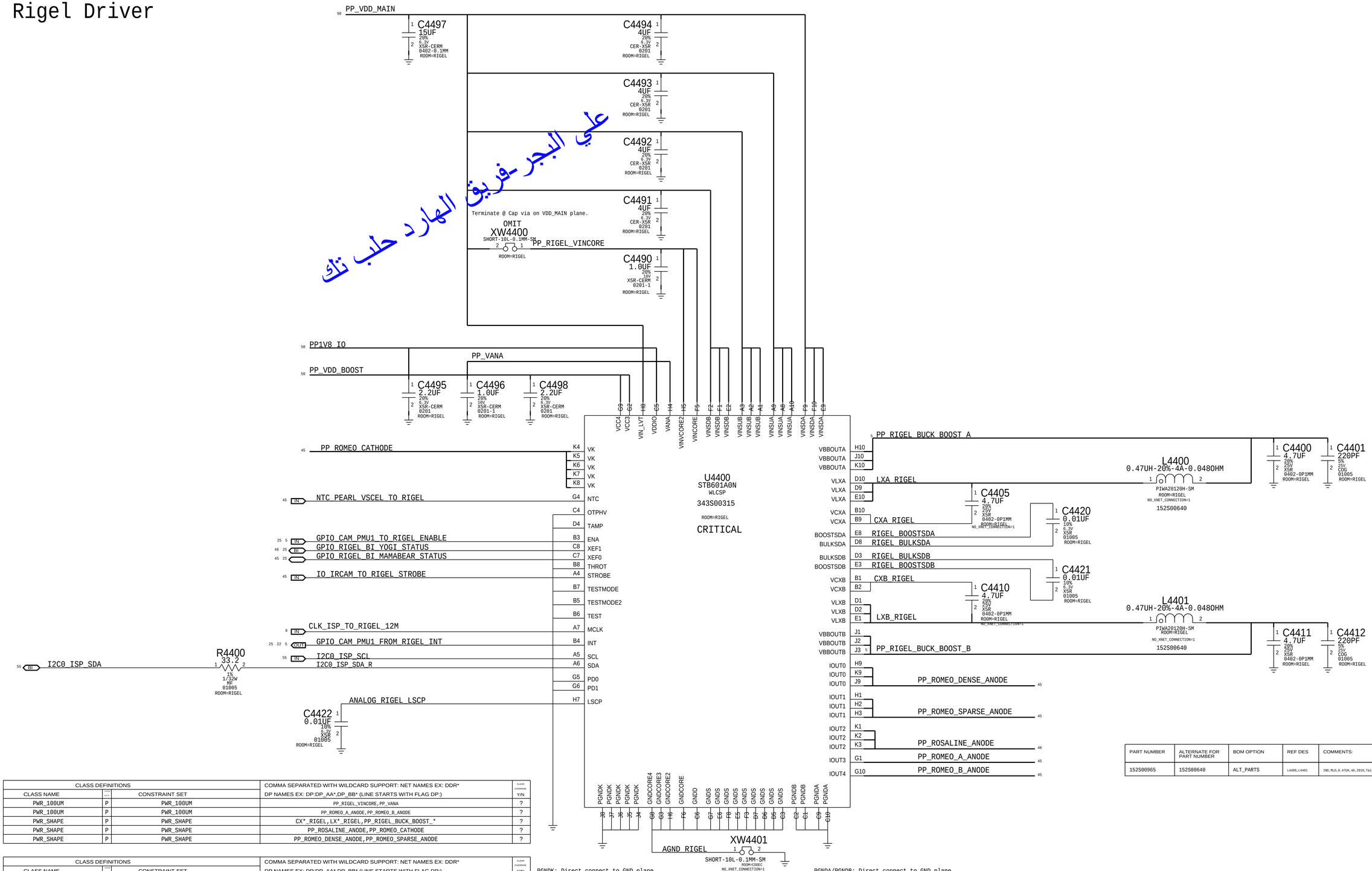


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01728	353S00015	ALT_PARTS	ALL	IC,LDO,REG,2.925V,250MA,ONSEMI

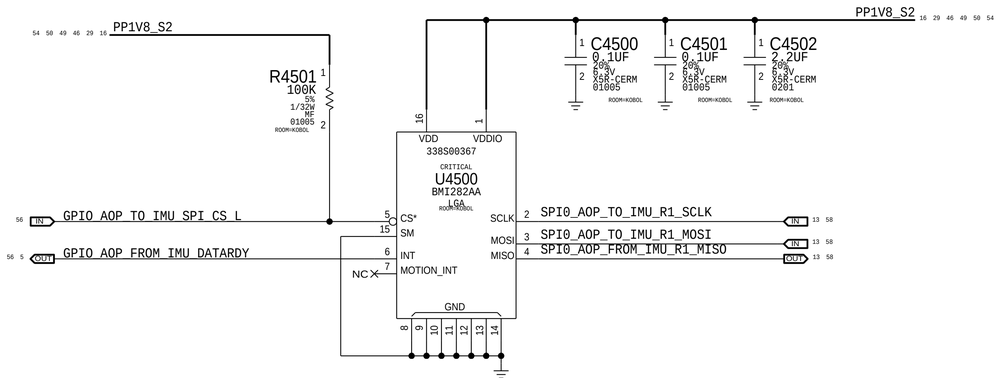
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_100UM	P	PWR_100UM	PP2V925_FCAM_AVDD	?
PWR_200UM	P	PWR_200UM	PP2V925_SWIDE_AVDD1	?
PWR_200UM	P	PWR_200UM	PP2V925_WIDE_AVDD1	?
PWR_200UM	P	PWR_200UM	PPVAR_TELE_AVDD2,PP2V925_TELE_AVDD1	?
PWR_200UM	P	PWR_200UM	PP3V3_RCAM_SVDD	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_100UM	S	100UM-249UM_SPACING	PP2V925_WIDE_AVDD*,PP2V925_FCAM_AVDD	?
S_PWR_200UM	S	100UM-249UM_SPACING	PP2V925_SWIDE_AVDD1	?
S_PWR_200UM	S	100UM-249UM_SPACING	PP2V925_TELE_AVDD1	?
S_PWR_200UM	S	100UM-249UM_SPACING	PP3V3_RCAM_SVDD	?

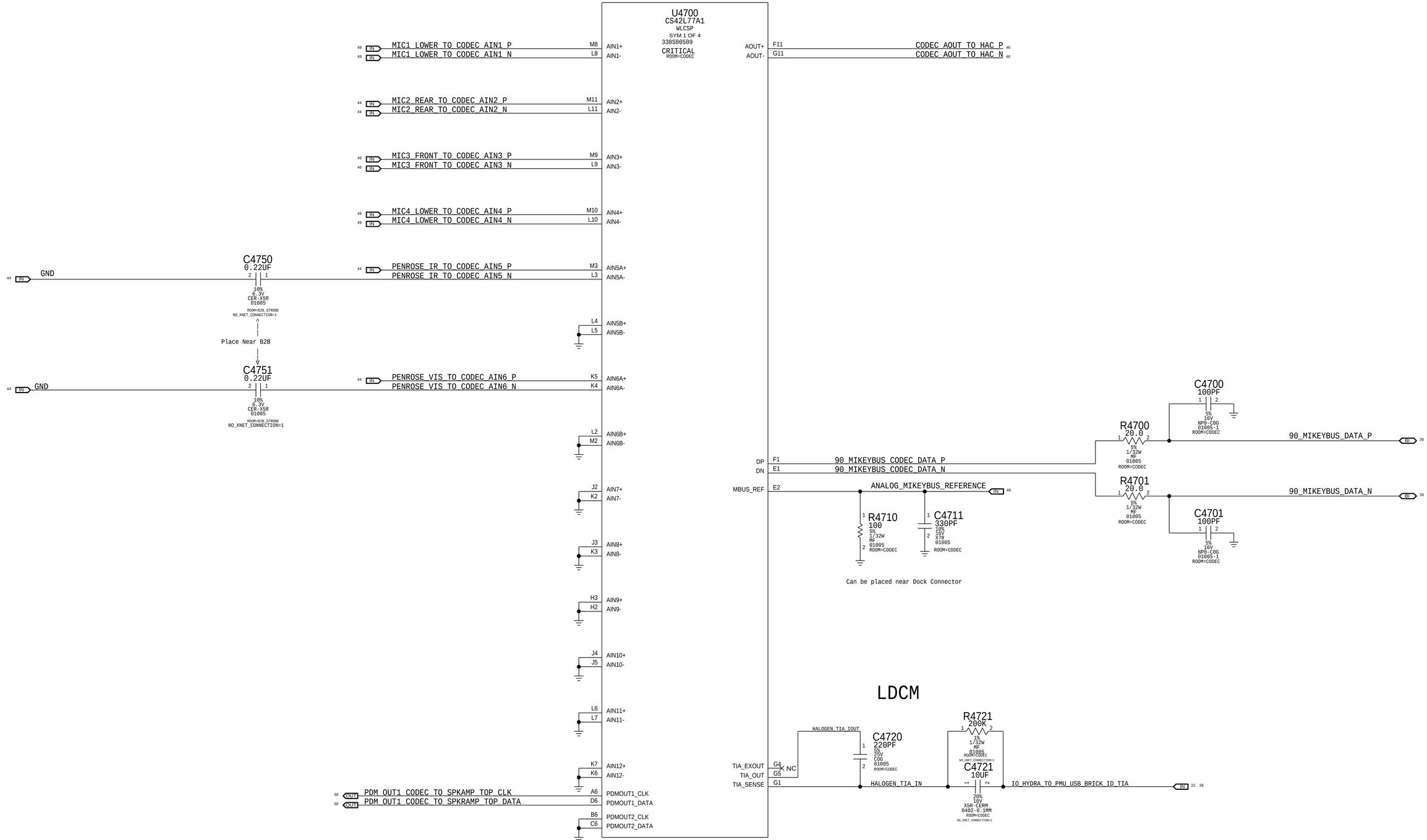
Rigel Driver


PP_VDD_MAIN
C4497 1.5UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=RIGEL
C4494 4UF 20% 6.3V CER-X5R 0201 ROOM=RIGEL
C4493 4UF 20% 6.3V CER-X5R 0201 ROOM=RIGEL
C4492 4UF 20% 6.3V CER-X5R 0201 ROOM=RIGEL
C4491 4UF 20% 6.3V CER-X5R 0201 ROOM=RIGEL
Terminate @ Cap via on VDD_MAIN plane.
OMIT
XW4400
SHORT-10L-0.1MM-SM
ROOM=RIGEL
PP_RIGEL_VINCORE
C4490 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=RIGEL
PP1V8_IO
PP_VANA
PP_VDD_BOOST
C4495 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=RIGEL
C4496 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=RIGEL
C4498 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=RIGEL
VCC4 VCC3 VIN_LVT VDDIO VANA VINVCORE2 VINCORE VINSDB VINSDB VINSDB VINSUB VINSUB VINSUB VINSUA VINSUA VINSUA VINSDA VINSDA VINSDA
PP_ROMEO_CATHODE
NTC_PEARL_VSCEL_TO_RIGEL
GPIO_CAM_PMU1_TO_RIGEL_ENABLE
GPIO_RIGEL_BI_YOGI_STATUS
GPIO_RIGEL_BI_MAMABEAR_STATUS
IO_IRCAM_TO_RIGEL_STROBE
CLK_ISP_TO_RIGEL_12M
GPIO_CAM_PMU1_FROM_RIGEL_INT
I2C0_ISP_SCL
I2C0_ISP_SDA_R
I2C0_ISP_SDA
R4400 33.2 1% 1/32W MF 01005 ROOM=RIGEL
ANALOG_RIGEL_LSCP
C4422 0.01UF 10% 6.3V X5R 01005 ROOM=RIGEL
VK VK VK VK VK
NTC
OTPHV
TAMP
ENA
XEF1
XEF0
THROT
STROBE
TESTMODE
TESTMODE2
TEST
MCLK
INT
SCL
SDA
PD0
PD1
LSCP
U4400
STB601A0N
WLCSP
343S00315
ROOM=RIGEL
CRITICAL
PGNDK PGNDK PGNDK PGNDK
GNDCORE4 GNDCORE3 GNDCORE2 GNDCORE GNDD GNDS GNDS GNDS

Kobol - Accel & Gyro



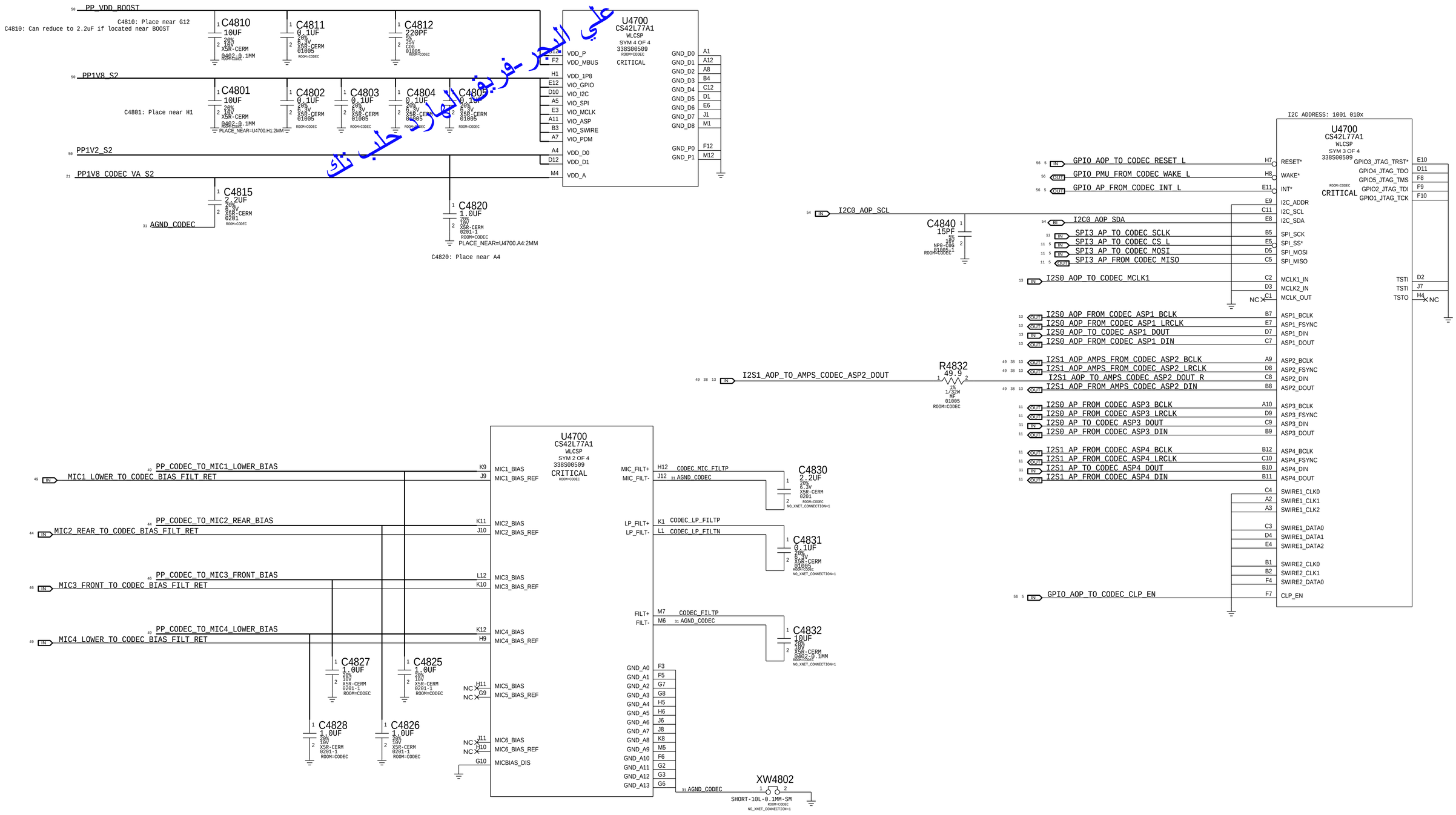
BRIGHTON AUDIO CODEC (ANALOG INPUTS & OUTPUTS)



CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	CLASS DEF.	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_80UM	P	PWR_80UM	PP1V8_CODEC_VA_S2	?
PWR_200UM	P	PWR_200UM	AGND_CODEC,CODEC_FILTP,CODEC_LP_FILTN	?

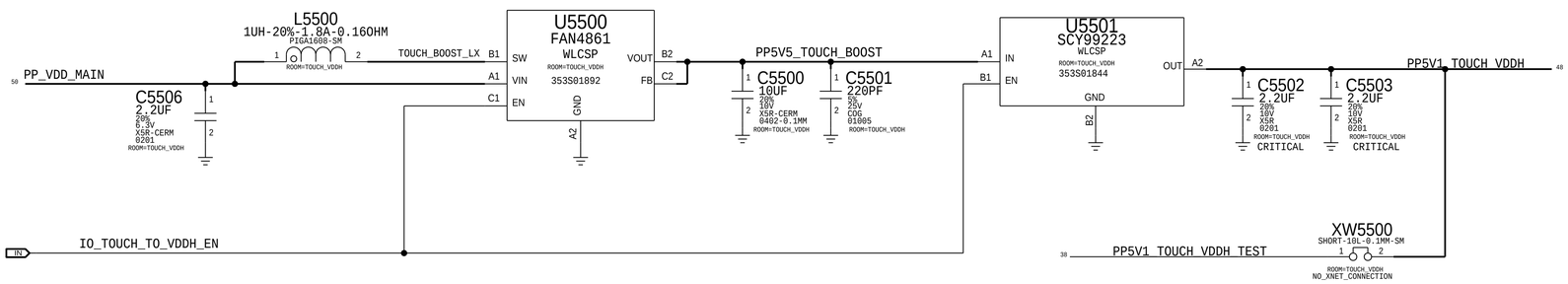
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	CLASS DEF.	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_200UM	S	100UM-249UM_SPACING	AGND_CODEC,CODEC_FILTP,CODEC_LP_FILTN	?

BRIGHTON AUDIO CODEC (POWER & I/O)



علي البحر فريق بهاء طب تك

TOUCH Discrete

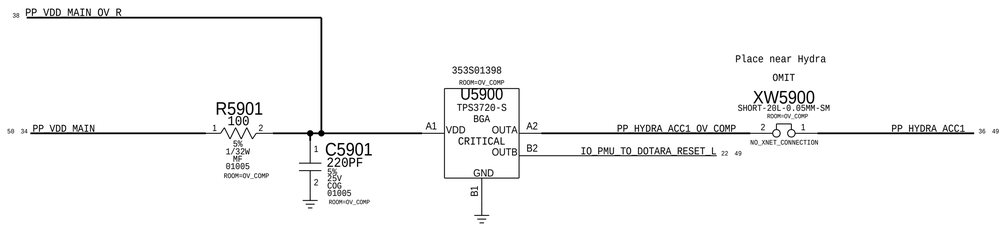


CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_100UM	P	PWR_100UM	PP5V1_TOUCH_VDDH_TEST	?
PWR_200UM	P	PWR_200UM	PP5V1_TOUCH_VDDH,PP5V5_TOUCH_BOOST	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_100UM	S	100UM-249UM_SPACING	PP5V1_TOUCH_VDDH_TEST	?
S_PWR_200UM	S	100UM-249UM_SPACING	PP5V1_TOUCH_VDDH,PP5V5_TOUCH_BOOST	?
SWITCHING	S	A_DIELECTRIC_1.5X	TOUCH_BOOST_LX	?

VDD_MAIN COMPARATORS

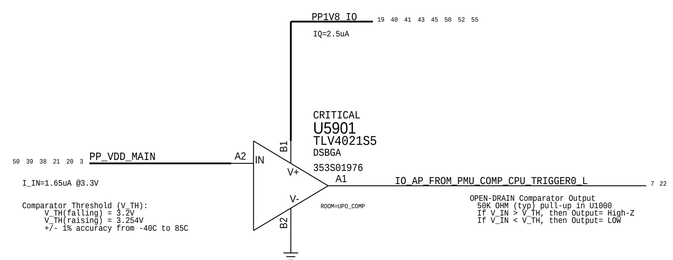
VDD_MAIN OV CUT-OFF CIRCUIT



Voltage Threshold = 5.2V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01375	353S01398	ALT_PARTS	U5900	ON SEMI

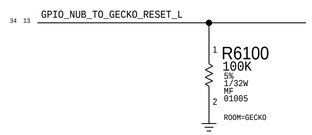
VDD_MAIN PRE-UPO COMPARATOR



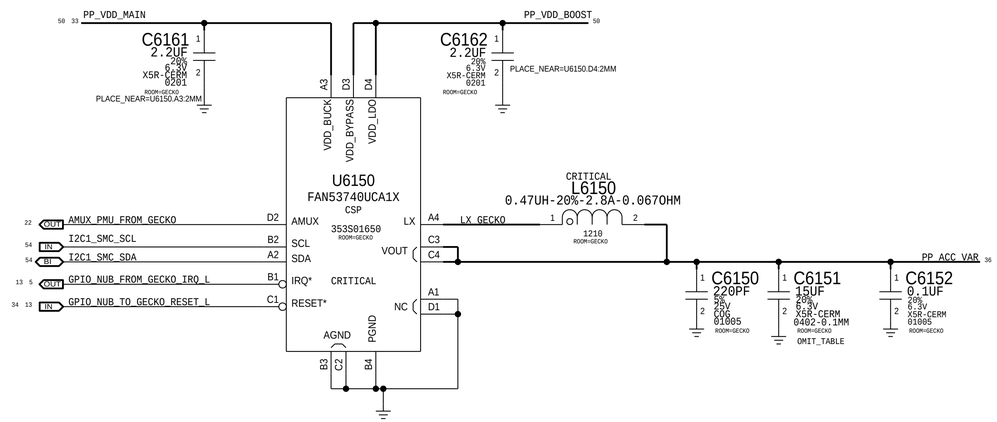
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR UNDERRIDE
CLASS NAME	CONST PRI	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_50UM	P	PWR_50UM	PP_VDD_MAIN_OV_R, PP_HYDRA_ACC1_OV_COMP	?

Gecko

GECKO Reset Pull Down



I2C ADDRESS: 0X52



IND Alternate

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00853	152S00854	ALT_PARTS	L6150	IND,PWR,0.47UH,20%,2.7A,TY

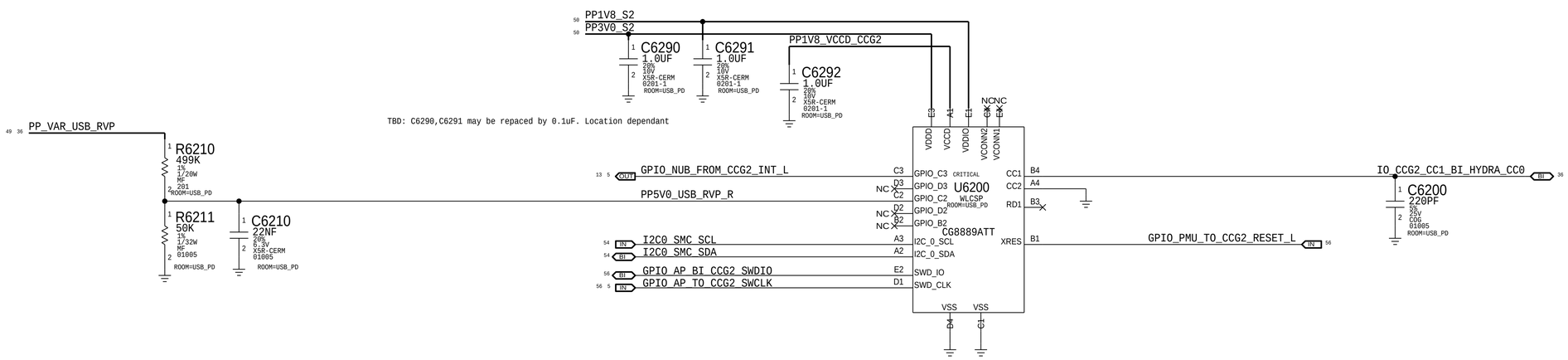
15uF Single Source

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S00003	1	CAP,15UF,6.3V,0402,MURATA	C6151	CRITICAL	CAP_15UF_SINGLE_SOURCE

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	CONST SET	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_SHAPE	P	PWR_SHAPE	LX_GECKO,PP_ACC_VAR	?

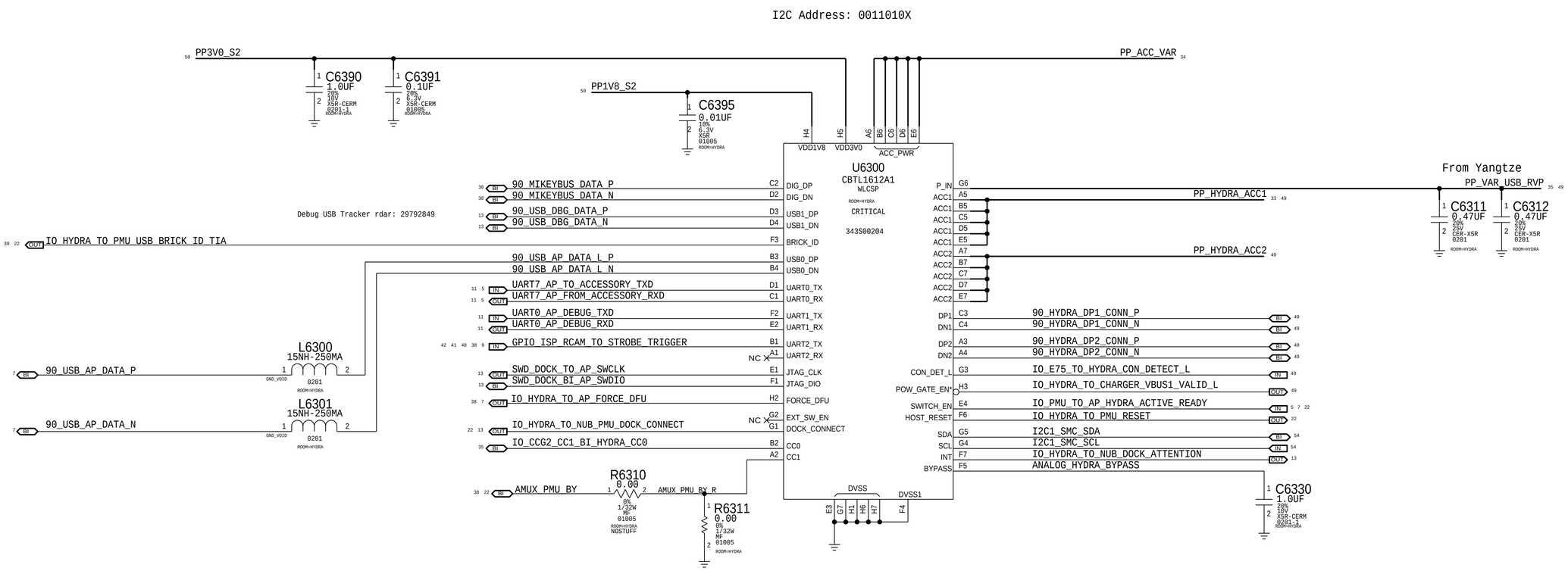
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	CONST SET	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_SHAPE	S	250UM+_SPACING	PP_ACC_VAR	?
SWITCHING	S	A_DIELECTRIC_1.5X	LX_GECKO	?

USB-PD



CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHARGED
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_80UM	P	PWR_80UM	PP1V8_VCCD_CCG2, PP5V0_USB_RVP_R	?

Hydra



CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_80UM	P	PWR_80UM	PP_VAR_USB_RVP	?
PWR_SHAPE	P	PWR_SHAPE	PP_HYDRA_ACC1,PP_HYDRA_ACC1_CONN,PP_HYDRA_ACC2*	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_SHAPE	S	250UM+_SPACING	PP_HYDRA_ACC*	?

OMIT

ROOM=B2B_INTERPOSER

998-18081

J_INT_BOT

SM

SYM 1 OF 3

INTERPOSER-MLB-DR-BOT-D4X

GND	1	IO1	IO95		GND
GND	2	IO2	IO96		GND
GND	3	IO3	IO97		90_PCIE4_AP_TO_BB_C_TX_N
GND	4	IO4	IO98	GND_VOID	GND
GND	5	IO5	IO99		90_PCIE4_AP_TO_BB_C_TX_P
GPIO_AP_CANARY2	6	IO6	IO100	GND_VOID	GND
GND	7	IO7	IO101		GND
NFC_ANT	8	IO8	IO102		GND
GND	9	IO9	IO103		GND
NFC_ANT	10	IO10	IO104		50_LAA_TO_XCVR_LAT
GND	11	IO11	IO105		GND
GND	12	IO12	IO106		GND
GND	13	IO13	IO107		50_WLAN_A_TX1
PP_VDD_MAIN	14	IO14	IO108		50_XCVR_TX1_HB
GND	15	IO15	IO109		GND
PP_VDD_MAIN	16	IO16	IO110		GND
GND	17	IO17	IO111		50_WLAN_A_RX1_LAA
GND	18	IO18	IO112		50_XCVR_TX1_MB1
GND	19	IO19	IO113		GND
PP_STROBE_DRIVER_COOL_LED	20	IO20	IO114		GND
GND	21	IO21	IO115		GND
PP_STROBE_DRIVER_WARM_LED	22	IO22	IO116		GND
GND	23	IO23	IO117		50_XCVR_TX0_MB2
GND	24	IO24	IO118		GND
GND	25	IO25	IO119		GND
GND	26	IO26	IO120		GND
GND	27	IO27	IO121		GND
GND	28	IO28	IO122		VPA_2G
GND	29	IO29	IO123		50_XCVR_TX1_UHB
GND	30	IO30	IO124		VPA_ET_UHB
GND	31	IO31	IO125		GND
GND	32	IO32	IO126		VPA_2G
GPIO_AP_FROM_BT_AUDIO_SYNC	33	IO33	IO127		VPA_ET_UHB
UART4_AP_FROM_NFC_CTS_L	34	IO34	IO128		GND
GPIO_AP_TO_NFC_DEV_WAKE	35	IO35	IO129		50_XCVR_TX0_MB3
UART4_AP_FROM_NFC_RXD	36	IO36	IO130		VPA_2G
GND	37	IO37	IO131		VPA_ET_UHB
UART4_AP_TO_NFC_TXD	38	IO38	IO132		GND
GND	39	IO39	IO133		50_XCVR_TX0_HB
SWD_AP_BI_BB_SWDIO	40	IO40	IO134		GND
GND	41	IO41	IO135		GND
UART4_AP_TO_NFC_RTS_L	42	IO42	IO136		GND
PP_GPU_LVCC	43	IO43	IO137		50_CPLL_CPLOUT2
UART2_AOP_FROM_BB_RXD	44	IO44	IO138		GND
GND	45	IO45	IO139		GND
SWD_NUB_TO_MANY_SWCLK	46	IO46	IO140		50_CPLL_CPLOUT1
PP_CPU_PCORE_LVCC	47	IO47	IO141		VPA_ET_HB
GPIO_AOP_FROM_HALL_CASE_INT_L	48	IO48	IO142		GND
GND	49	IO49	IO143		GND
GPIO_AOP_FROM_NFC_HOST_WAKE	50	IO50	IO144		GND
I2C2_AP_SCL	51	IO51	IO145		GND
GND	52	IO52	IO146		GND
UART2_AOP_TO_BB_TXD	53	IO53	IO147		VPA_ET_HB
GND	54	IO54	IO148		GND
GND	55	IO55	IO149		GND
GND	56	IO56	IO150		GND
GND	57	IO57	IO151		GND
GND	58	IO58	IO152		GND
GND	59	IO59	IO153		VPA_ET_HB
GND	60	IO60	IO154		GND
SPMI1_AOP_TO_RF_CLK	61	IO61	IO155		GND
GND	62	IO62	IO156		GND
SPMI1_AOP_BI_RF_DATA	63	IO63	IO157		GND
GND	64	IO64	IO158		GND
GND	65	IO65	IO159		GND
GND	66	IO66	IO160		GND
90_PCIE3_AP_TO_WLAN_REFCLK_N	67	IO67	IO161		GND
GND	68	IO68	IO162		GND
90_PCIE3_AP_TO_WLAN_REFCLK_P	69	IO69	IO163		GND
GND	70	IO70	IO164		GND
GND	71	IO71	IO165		GND
GND	72	IO72	IO166		GND
90_PCIE4_AP_TO_BB_REFCLK_P	73	IO73	IO167		GND
GND	74	IO74	IO168		GND
90_PCIE4_AP_TO_BB_REFCLK_N	75	IO75	IO169		GPIO_AP_CANARY1
GND	76	IO76	IO170		GND
GND	77	IO77	IO171		50_XCVR_RX6_MB_UHB_PRX
GND	78	IO78	IO172		GND
90_PCIE3_AP_TO_WLAN_C_TX_P	79	IO79	IO173		GND
GND	80	IO80	IO174		GND
90_PCIE3_AP_TO_WLAN_C_TX_N	81	IO81	IO175		GND
GND	82	IO82	IO176		GND
GND	83	IO83	IO177		50_XCVR_RX10_MLB_HB_PRX
GND	84	IO84	IO178		LAT_SAWTOOTH_A
90_PCIE3_AP_FROM_WLAN_C_RX_N	85	IO85	IO179		GND
GND	86	IO86	IO180		GND
90_PCIE3_AP_FROM_WLAN_C_RX_P	87	IO87	IO181		GND
GND	88	IO88	IO182		GND
GND	89	IO89	IO183		RFA1_SW_CTRL0
GND	90	IO90	IO184		50_HBPA_DRX_OUT
90_PCIE4_AP_FROM_BB_C_RX_N	91	IO91	IO185		GND
GND	92	IO92	IO186		GND
90_PCIE4_AP_FROM_BB_C_RX_P	93	IO93	IO187		GND
GND	94	IO94	IO188		50_MMDSM_MHB_ANT

998-18081

J_INT_BOT

SM

SYM 2 OF 3

INTERPOSER-MLB-DR-BOT-D4X

GND	189	IO189	IO283		PP_VDD_MAIN
GND	190	IO190	IO284		PP_VDD_MAIN
GND	191	IO191	IO285		PP_VDD_MAIN
GND	192	IO192	IO286		PP_VDD_MAIN
RFFE_XCVR_TO_LBTX_CLK	193	IO193	IO287		PDM_OUT1_CODEC_TO_SPKAMP_TOP_CLK
RFFE_XCVR_TO_LBTX_DATA	194	IO194	IO288		GND
GND	195	IO195	IO289		I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK
GND	196	IO196	IO290		GPIO_AP_FROM_SPKRAMP_TOP_INT_L
GND	197	IO197	IO291		I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN
GND	198	IO198	IO292		GND
RFA1_SW_CTRL2	199	IO199	IO293		I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK
VFE_LO_1V2	200	IO200	IO294		GPIO_AP_TO_SPKRAMP_TOP_RESET_L
GND	201	IO201	IO295		PDM_OUT1_CODEC_TO_SPKRAMP_TOP_DATA
50_XCVR_RX2_UHB_PRX	202	IO202	IO296		GND
GND	203	IO203	IO297		PP1V2_S2
GND	204	IO204	IO298		GPIO_AOP_TO_WLAN_CONTEXT_A
GND	205	IO205	IO299		PP1V8_S2
50_UHBPA_UHB	206	IO206	IO300		GND
GND	207	IO207	IO301		I2C2_AP_SDA
GND	208	IO208	IO302		GPIO_AOP_TO_WLAN_CONTEXT_B
GND	209	IO209	IO303		GPIO_TOUCH_TO_MANY_SCAN_ACTIVE
5GHZ_C1_VDET	210	IO210	IO304		GND
GND	211	IO211	IO305		I2C_R1_BI_NFC_SDA
RFA1_SW_CTRL1	212	IO212	IO306		GND
GND	213	IO213	IO307		GND
GND	214	IO214	IO308		IO_BB_TO_R1_COEX
IO_PMU_TO_SYSTEM_RESET_L	215	IO215	IO309		GND
I2S2_AP_TO_BB_DOUT	216	IO216	IO310		GND
GND	217	IO217	IO311		IO_R1_TO_WLAN_COEX
I2S2_AP_FROM_BB_DIN	218	IO218	IO312		I2C_R1_TO_NFC_SCL
GPIO_NUB_TO_BBPMU_CLK_EN	219	IO219	IO313		GND
I2S2_AP_FROM_BB_BCLK	220	IO220	IO314		GND
GND	221	IO221	IO315		GND
I2S2_AP_FROM_BB_LRCLK	222	IO222	IO316		GND
GPIO_AP_FROM_BB_RESET_DETECT_1V2	223	IO223	IO317		GND
I2S0_AP_TO_SPKAMP_TOP_MCLK	224	IO224	IO318		GND
GND	225	IO225	IO319		GND
GPIO_AP_TO_BB_COREDUMP_1V2	226	IO226	IO320		IO_TOUCH_TO_VDDH_EN
PCIE4_AP_TO_BB_PERST_1V2_L	227	IO227	IO321		IO_WLAN_TO_R1_COEX
GND	228	IO228	IO322		PP5V1_TOUCH_VDDH_TEST
PCIE3_AP_BI_WLAN_CLKREQ_1V2_L	229	IO229	IO323		GPIO_BT_TO_R1_DEV_WAKE
GPIO_AP_FROM_WLAN_TIME_SYNC_1V2	230	IO230	IO324		GND
PCIE3_AP_TO_WLAN_PERST_1V2_L	231	IO231	IO325		IO_BT_TO_R1_TIME_SYNC
GND	232	IO232	IO326		SPKRAMP_TOP_TO_COIL_OUT_POS
GND	233	IO233	IO327		GND
PCIE4_AP_BI_BB_CLKREQ_1V2_L	234	IO234	IO328		COIL_TO_SPKRAMP_TOP_VSENSE_POS
GND	235	IO235	IO329		SPKRAMP_TOP_TO_COIL_OUT_POS
GND	236	IO236	IO330		COIL_TO_SPKRAMP_TOP_VSENSE_NEG
CLK_BBPMU_TO_DOTARA_38M4_1V8	237	IO237	IO331		GND
GND	238	IO238	IO332		SPKRAMP_TOP_TO_COIL_OUT_NEG
IO_SPKAMP_TO_SPKAMP_SYNC	239	IO239	IO333		SPKRAMP_TOP_TO_COIL_OUT_NEG
GND	240	IO240	IO334		GND
GND	241	IO241	IO335		GND
IO_BT_TO_BOT_SPK_TRIG	242	IO242	IO336		RFFE_LAA_UAT_VIO
GND	243	IO243	IO337		RFFE_LAA_UAT_CLK
GND	244	IO244	IO338		GND
GND	245	IO245	IO339		RFFE_LAA_UAT_DATA
GND	246	IO246	IO340		5GHZ_C0_VDET
NTC_RADIO_BB_N	247	IO247	IO341		GND
GND	248	IO248	IO342		GND
NTC_RADIO_BB_P	249	IO249	IO343		50_WLAN_A_TX0
GND	250	IO250	IO344		GND
GND	251	IO251	IO345		GND
GND	252	IO252	IO346		50_WLAN_A_RX0_LAA
PP_VDD_MAIN_OV_R	253	IO253	IO347		GND
GND	254	IO254	IO348		GND
GND	255	IO255	IO349		50_LAA_TO_XCVR_UAT
GND	256	IO256	IO350		GND
IO_NFC_TO_ARC_RESET_L	257	IO257	IO351		GND
GND	258	IO258	IO352		GND
GND	259	IO259	IO353		RFA0_SW_CTRL2
IO_NFC_TO_ARC_TRIG	260	IO260	IO354		GND
GPIO_PMU_FROM_CHARGER_INT_L	261	IO261	IO355		GND
I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT	262	IO262	IO356		GND
GND	263	IO263	IO357		IO_R1_TO_BB_LAA_SW_CTRL
IO_HYDRA_TO_AP_FORCE_DFU	264	IO264	IO358		GND
GND	265	IO265	IO359		RFA0_SW_CTRL1
GND	266	IO266	IO360		GND
GND	267	IO267	IO361		GND
GND	268	IO268	IO362		RFA0_SW_CTRL0
GND	269	IO269	IO363		GND
GND	270	IO270	IO364		GND
GND	271	IO271	IO365		GND
GND	272	IO272	IO366		GND
GND	273	IO273	IO367		GND
GND	274	IO274	IO368		GND
GND	275	IO275	IO369		GND
GND	276	IO276	IO370		GND
GND	277	IO277	IO371		UAT_SAWTOOTH_B
GND	278	IO278	IO372		GND
GND	279	IO279	IO373		UAT_SAWTOOTH_A
GND	280	IO280	IO374		GND
GND	281	IO281	IO375		GND
PP_VDD_MAIN	282	IO282	IO376		GND

998-18081

J_INT_BOT

SM

SYM 3 OF 3

INTERPOSER-MLB-DR-BOT-D4X

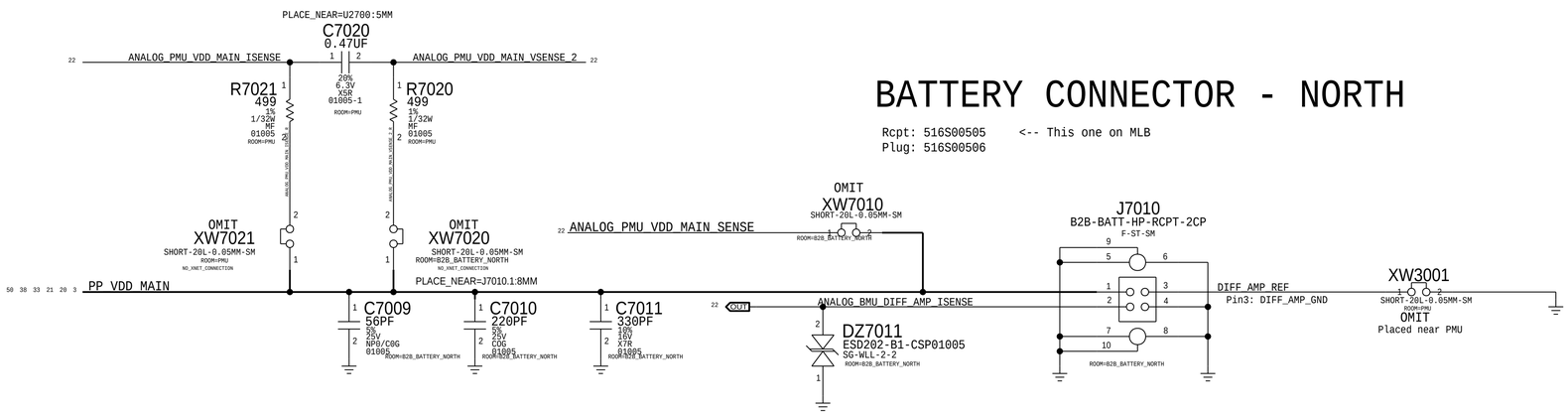
50_ANT4	377	IO377	IO461	461	50_UHBPA_2G_LB_OUT
GND	378	IO378	IO462	462	GND
GND	379	IO379	IO463	463	GND
GND	380	IO380	IO464	464	50_WLAN_G_LAT
50_ANT2	381	IO381	IO465	465	GND
GND	382	IO382	IO466	466	GND
GND	383	IO383	IO467	467	GND
GND	384	IO384	IO468	468	50_MMDSM_UHB_ANT
50_ANT6_UHB	385	IO385	IO469	469	GND
GND	386	IO386	IO470	470	50_LB_TX_ANT1
GND	387	IO387	IO471	471	GND
GND	388	IO388	IO472	472	GND
GND	389	IO389	IO473	473	GND
GND	390	IO390	IO474	474	LAT_SAWTOOTH_B
GND	391	IO391	IO475	475	GND
GND	392	IO392	IO476	476	GND
GND	393	IO393	IO477	477	GND
GND	394	IO394	IO478	478	GND
GND	395	IO395	IO479	479	GND
GND	396	IO396	IO480	480	GND
PP1V2_S4	397	IO397	IO481	481	GND
GND	398	IO398	IO482	482	50_XCVR_RX14_LB_MLB_PRX
GND	399	IO399	IO483	483	GND
GND	400	IO400	IO484	484	GND
GND	401	IO401	IO485	485	VIO_RFFE_XCVR_TO_RX_1V8
GND	402	IO402	IO486	486	RFFE_XCVR_TO_FE_RX_DATA
GND	403	IO403	IO487	487	RFFE_XCVR_TO_FE_RX_CLK
GND	404	IO404	IO488	488	VIO_RFFE_XCVR_TO_TX_1V8
GND	405	IO405	IO489	489	RFFE_XCVR_TO_HBTX_DATA
GPIO_PMU_TO_WLAN_REG_ON	406	IO406	IO490	490	RFFE_XCVR_TO_HBTX_CLK
GND	407	IO407	IO491	491	GND
GND	408	IO408	IO492	492	VFE_HI_3V15
GND	409	IO409	IO493	493	GND
GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L	410	IO410	IO494	494	GND
I2C2_CAM_PMU1_SCL	411	IO411	IO495	495	50_HBPA_ANT3
GND	412	IO412	IO496	496	GND
I2C2_CAM_PMU1_SDA	413	IO413	IO497	497	GND
PP1V8_S4	414	IO414	IO498	498	50_XCVR_RX8_MLB_HB_PRX
PP1V8_NFC_S2	415	IO415	IO499	499	GND
GND	416	IO416	IO500	500	GND
AMUX_PMU_AY	417	IO417	IO501	501	50_XCVR_RX9_MLB_HB_PRX
GPIO_PMU_FROM_WLAN_HOST_WAKE	418	IO418	IO502	502	GND
GPIO_ISP_RCAM_TO_STROBE_TRIGGER	419	IO419	IO503	503	GND
GND	420	IO420	IO504	504	GND
GPIO_BB_TO_MANY_GSM_BURST_IND	421	IO421	IO505	505	GND
GPIO_PMU_TO_BBPMU_RESET_L	422	IO422	IO506	506	GND
GPIO_CAM_PMU1_TO_STROBE_DRIVER_HWEN	423	IO423			
GND	424	IO424			
CLK_GPIO_PMU_TO_WLAN_R1_32K	425	IO425			
GPIO_PMU_TO_NFC_EN	426	IO426			
NTC_STROBE_MODULE	427	IO427			
GND	428	IO428			
GND	429	IO429			
AMUX_PMU_BY	430	IO430			
GND	431	IO431			
GND	432	IO432			
GND	433	IO433			
GND	434	IO434			
GND	435	IO435			
GND	436	IO436			
GND	437	IO437			
GND	438	IO438			
GND	439	IO439			
GND	440	IO440			
GND	441	IO441			
GND	442	IO442			
GND	443	IO443			
GND	444	IO444			
GND	445	IO445			
50_XCVR_TX0_LB2	446	IO446			
GND	447	IO447			
GND	448	IO448			
50_XCVR_TX0_MB1	449	IO449			
GND	450	IO450			
GND	451	IO451			
GND	452	IO452			
GND	453	IO453			
GND	454	IO454			
GND	455	IO455			
GND	456	IO456			
GND	457	IO457			
GND	458	IO458			
GND	459	IO459			
GND	460	IO460			

37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GPIO_AP_CANARY2	MAKE_BASE=TRUE	GPIO_AP_CANARY2	56	
37	GND	MAKE_BASE=TRUE	GND		
37	NFC_ANT	MAKE_BASE=TRUE	NFC_ANT	38	44
37	GND	MAKE_BASE=TRUE	GND		
37	NFC_ANT	MAKE_BASE=TRUE	NFC_ANT	38	44
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	BP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	3 20 21 33 38 39 50	
37	GND	MAKE_BASE=TRUE	GND		
37	BP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	3 20 21 33 38 39 50	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	BP_STROBE_DRIVER_COOL_LED	MAKE_BASE=TRUE	PP_STROBE_DRIVER_COOL_LED	44	
37	GND	MAKE_BASE=TRUE	GND		
37	BP_STROBE_DRIVER_WARM_LED	MAKE_BASE=TRUE	PP_STROBE_DRIVER_WARM_LED	44	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GPIO_AP_FROM_BT_AUDIO_SYNC	MAKE_BASE=TRUE	GPIO_AP_FROM_BT_AUDIO_SYNC	56	
37	UART4_AP_FROM_NFC_CTS_L	MAKE_BASE=TRUE	UART4_AP_FROM_NFC_CTS_L	11	
37	GPIO_AP_TO_NFC_DEV_WAKE	MAKE_BASE=TRUE	GPIO_AP_TO_NFC_DEV_WAKE	56	
37	UART4_AP_FROM_NFC_RXD	MAKE_BASE=TRUE	UART4_AP_FROM_NFC_RXD	11	
37	GND	MAKE_BASE=TRUE	GND		
37	UART4_AP_TO_NFC_TXD	MAKE_BASE=TRUE	UART4_AP_TO_NFC_TXD	11	
37	GND	MAKE_BASE=TRUE	GND		
37	SWD_AP_BI_BB_SWDIO	MAKE_BASE=TRUE	SWD_AP_BI_BB_SWDIO	7	
37	GND	MAKE_BASE=TRUE	GND		
37	UART4_AP_TO_NFC_RTS_L	MAKE_BASE=TRUE	UART4_AP_TO_NFC_RTS_L	11	
37	BP_GPU_LVCC	MAKE_BASE=TRUE	PP_GPU_LVCC	5	
37	UART2_AOP_FROM_BB_RXD	MAKE_BASE=TRUE	UART2_AOP_FROM_BB_RXD	13	
37	GND	MAKE_BASE=TRUE	GND		
37	SWD_NUB_TO_MANY_SWCLK	MAKE_BASE=TRUE	SWD_NUB_TO_MANY_SWCLK	13 18 22 58	
37	BP_CPU_PCORE_LVCC	MAKE_BASE=TRUE	PP_CPU_PCORE_LVCC	5	
37	GPIO_AOP_FROM_HALL_CASE_INT_L	MAKE_BASE=TRUE	GPIO_AOP_FROM_HALL_CASE_INT_L	56	
37	GND	MAKE_BASE=TRUE	GND		
37	GPIO_AOP_FROM_NFC_HOST_WAKE	MAKE_BASE=TRUE	GPIO_AOP_FROM_NFC_HOST_WAKE	56	
37	I2C2_AP_SCL	MAKE_BASE=TRUE	I2C2_AP_SCL	11 53	
37	GND	MAKE_BASE=TRUE	GND		
37	UART2_AOP_TO_BB_TXD	MAKE_BASE=TRUE	UART2_AOP_TO_BB_TXD	13	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	SPMI1_AOP_TO_RF_CLK	MAKE_BASE=TRUE	SPMI1_AOP_TO_RF_CLK	13	
37	GND	MAKE_BASE=TRUE	GND		
37	SPMI1_AOP_BI_RF_DATA	MAKE_BASE=TRUE	SPMI1_AOP_BI_RF_DATA	13	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE3_AP_TO_WLAN_REFCLK_N	MAKE_BASE=TRUE	90_PCIE3_AP_TO_WLAN_REFCLK_N	8	
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE3_AP_TO_WLAN_REFCLK_P	MAKE_BASE=TRUE	90_PCIE3_AP_TO_WLAN_REFCLK_P	8	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE4_AP_TO_BB_REFCLK_P	MAKE_BASE=TRUE	90_PCIE4_AP_TO_BB_REFCLK_P	8	
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE4_AP_TO_BB_REFCLK_N	MAKE_BASE=TRUE	90_PCIE4_AP_TO_BB_REFCLK_N	8	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE3_AP_TO_WLAN_C_TX_P	MAKE_BASE=TRUE	90_PCIE3_AP_TO_WLAN_C_TX_P	8	
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE3_AP_TO_WLAN_C_TX_N	MAKE_BASE=TRUE	90_PCIE3_AP_TO_WLAN_C_TX_N	8	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE3_AP_FROM_WLAN_C_RX_N	MAKE_BASE=TRUE	90_PCIE3_AP_FROM_WLAN_C_RX_N	8	
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE3_AP_FROM_WLAN_C_RX_P	MAKE_BASE=TRUE	90_PCIE3_AP_FROM_WLAN_C_RX_P	8	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE4_AP_FROM_BB_C_RX_N	MAKE_BASE=TRUE	90_PCIE4_AP_FROM_BB_C_RX_N	8	
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE4_AP_FROM_BB_C_RX_P	MAKE_BASE=TRUE	90_PCIE4_AP_FROM_BB_C_RX_P	8	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE4_AP_TO_BB_C_TX_N	MAKE_BASE=TRUE	90_PCIE4_AP_TO_BB_C_TX_N	8	
37	GND	MAKE_BASE=TRUE	GND		
37	90_PCIE4_AP_TO_BB_C_TX_P	MAKE_BASE=TRUE	90_PCIE4_AP_TO_BB_C_TX_P	8	
37	GND	MAKE_BASE=TRUE	GND		

37	GND	MAKE_BASE=TRUE	GND		
37	50_XCVR_RX2_UHB_PRX	MAKE_BASE=TRUE	50_XCVR_RX2_UHB_PRX	58	
37	GND	MAKE_BASE=TRUE	GND		
37	50_LAA_TO_XCVR_LAT	MAKE_BASE=TRUE	50_LAA_TO_XCVR_LAT	58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	50_WLAN_A_TX1	MAKE_BASE=TRUE	50_WLAN_A_TX1	58	
37	50_XCVR_TX1_HB	MAKE_BASE=TRUE	50_XCVR_TX1_HB	58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	50_WLAN_A_RX1_LAA	MAKE_BASE=TRUE	50_WLAN_A_RX1_LAA	58	
37	50_XCVR_TX1_MB1	MAKE_BASE=TRUE	50_XCVR_TX1_MB1	58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	50_XCVR_TX0_MB2	MAKE_BASE=TRUE	50_XCVR_TX0_MB2	58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	VPA_2G	MAKE_BASE=TRUE	VPA_2G	38 58	
37	50_XCVR_TX1_UHB	MAKE_BASE=TRUE	50_XCVR_TX1_UHB	58	
37	VPA_ET_UHB	MAKE_BASE=TRUE	VPA_ET_UHB	38 58	
37	GND	MAKE_BASE=TRUE	GND		
37	VPA_2G	MAKE_BASE=TRUE	VPA_2G	38 58	
37	VPA_ET_UHB	MAKE_BASE=TRUE	VPA_ET_UHB	38 58	
37	GND	MAKE_BASE=TRUE	GND		
37	50_XCVR_TX0_MB3	MAKE_BASE=TRUE	50_XCVR_TX0_MB3	58	
37	VPA_2G	MAKE_BASE=TRUE	VPA_2G	38 58	
37	VPA_ET_UHB	MAKE_BASE=TRUE	VPA_ET_UHB	38 58	
37	GND	MAKE_BASE=TRUE	GND		
37	50_XCVR_TX0_HB	MAKE_BASE=TRUE	50_XCVR_TX0_HB	58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	50_CPLL_CPLOUT2	MAKE_BASE=TRUE	50_CPLL_CPLOUT2	58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	50_CPLL_CPLOUT1	MAKE_BASE=TRUE	50_CPLL_CPLOUT1	58	
37	VPA_ET_HB	MAKE_BASE=TRUE	VPA_ET_HB	38 58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	VPA_ET_HB	MAKE_BASE=TRUE	VPA_ET_HB	38 58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	VPA_ET_HB	MAKE_BASE=TRUE	VPA_ET_HB	38 58	
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND		
37	GND	MAKE_BASE=TRUE	GND

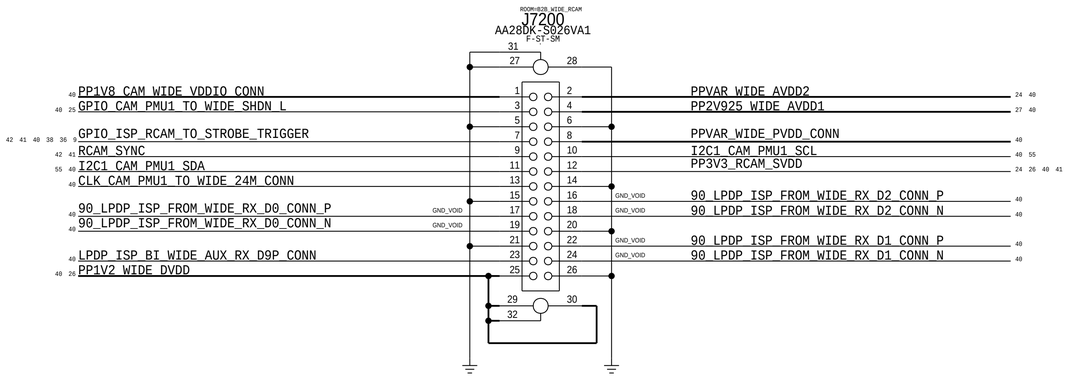
BATTERY CONNECTOR - NORTH

Rcpt: 516S00505 <-- This one on MLB
Plug: 516S00506



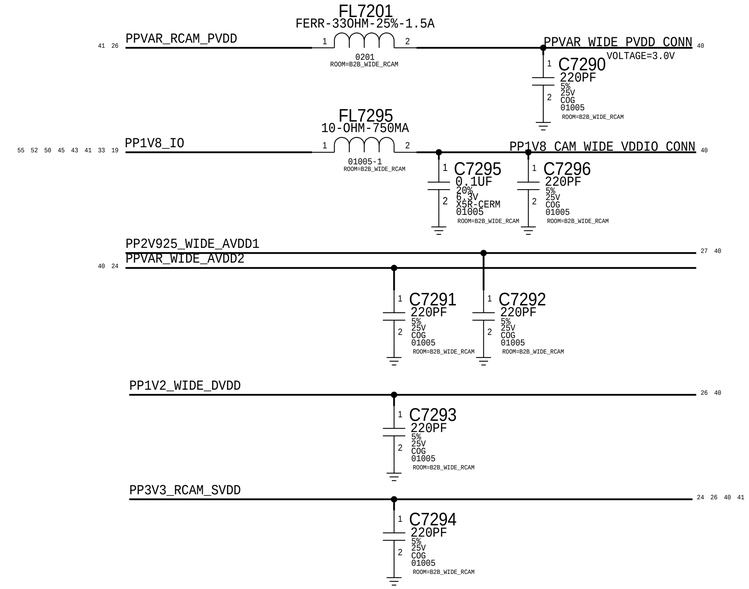
Wide Camera Connector

Rcpt: 516S00402 <-- This one on MLB
Plug: 516S00403

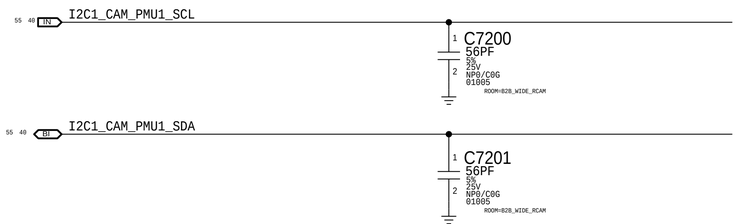


Pin Assignments based on D42 (flex_rcam_on_l_0.5.0)

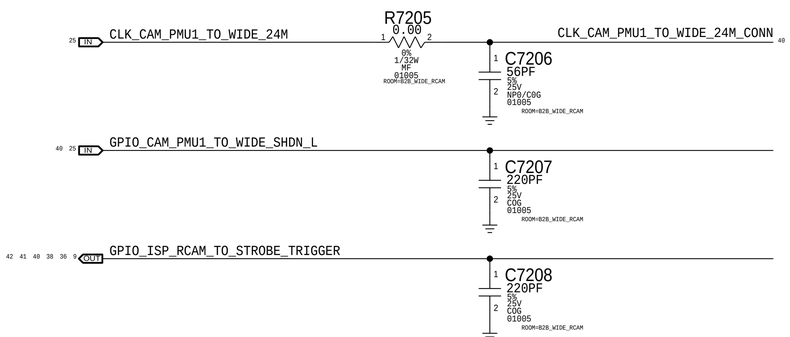
Power Filtering



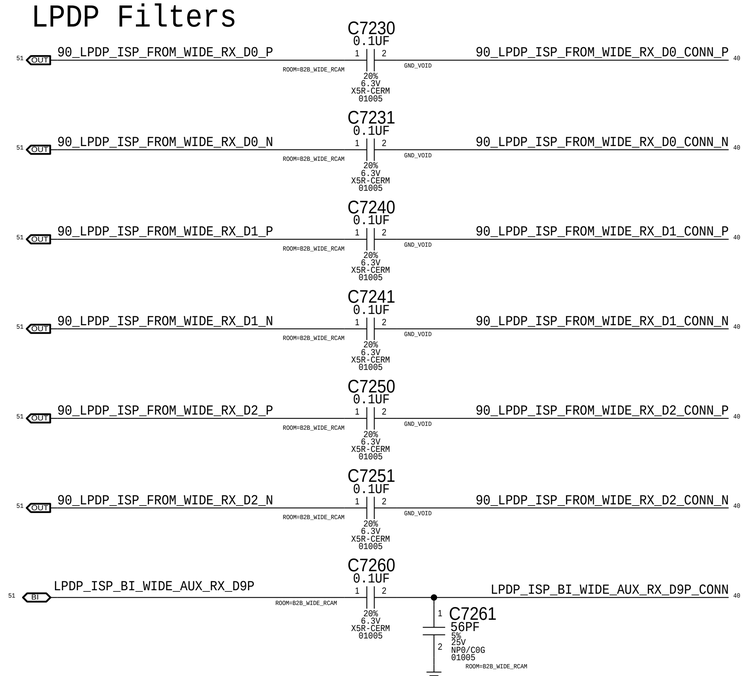
CAM_PMU1 I2C1



IO Filters



LPDP Filters

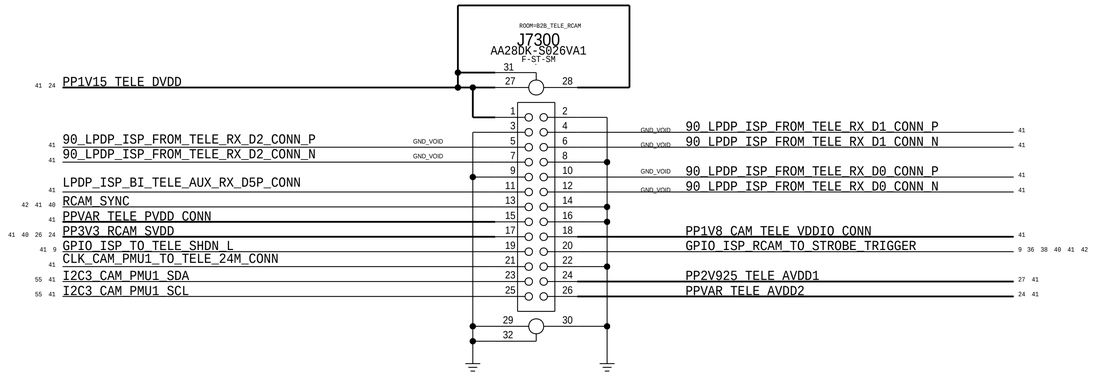


CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS CHANGE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*.DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_100UM	P	PWR_100UM	PP1V8_CAM_WIDE_VDDIO_CONN	?
PWR_SHAPE	P	PWR_SHAPE	PPVAR_WIDE_PVDD_CONN	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS CHANGE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*.DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_100UM	S	100UM-249UM_SPACING	PP1V8_CAM_WIDE_VDDIO_CONN	?
S_PWR_SHAPE	S	250UM+_SPACING	PPVAR_WIDE_PVDD_CONN	?

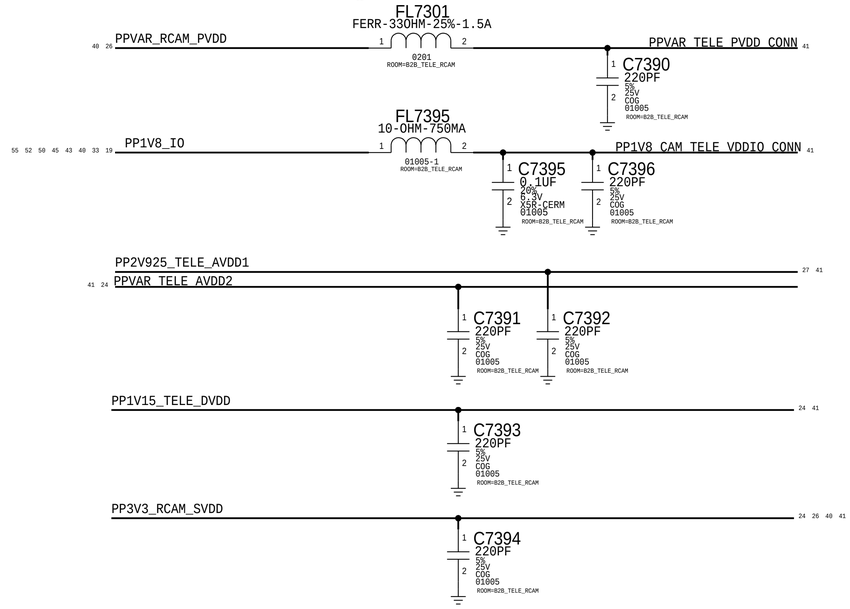
Tele Camera Connector

Rcpt: 516S00402 <-- This one on MLB
Plug: 516S00403

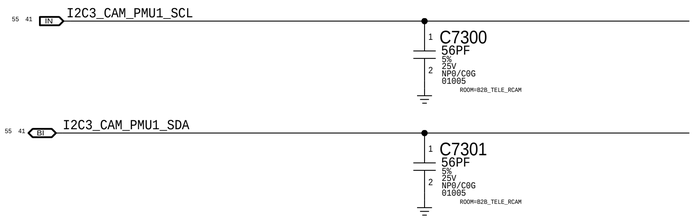


Pin Assignments based on D42 (flex_rcam_ab_l_0.3.0)

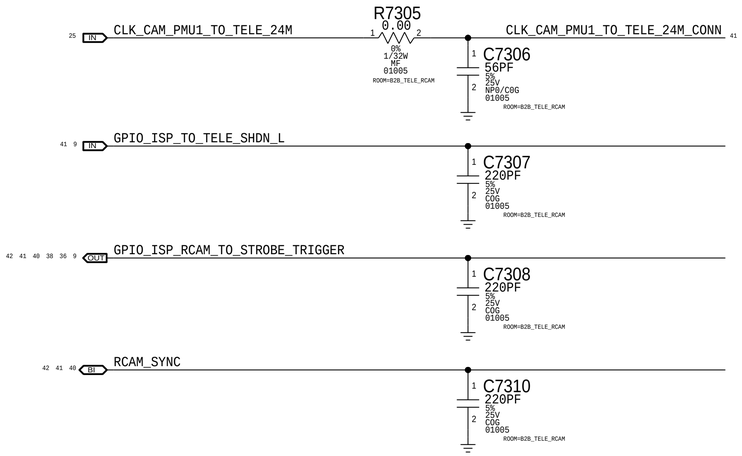
Power Filtering



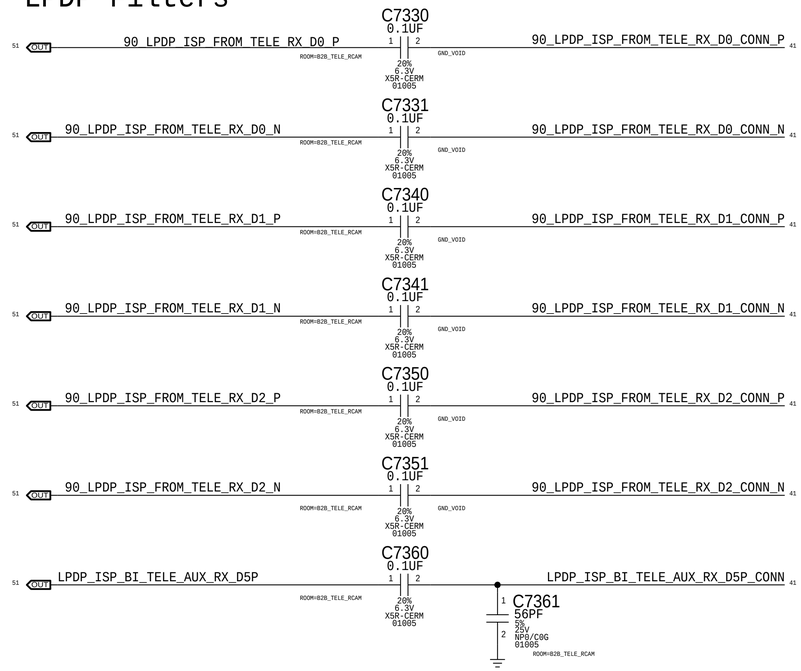
CAM_PMU1 I2C3



IO Filters



LPDP Filters

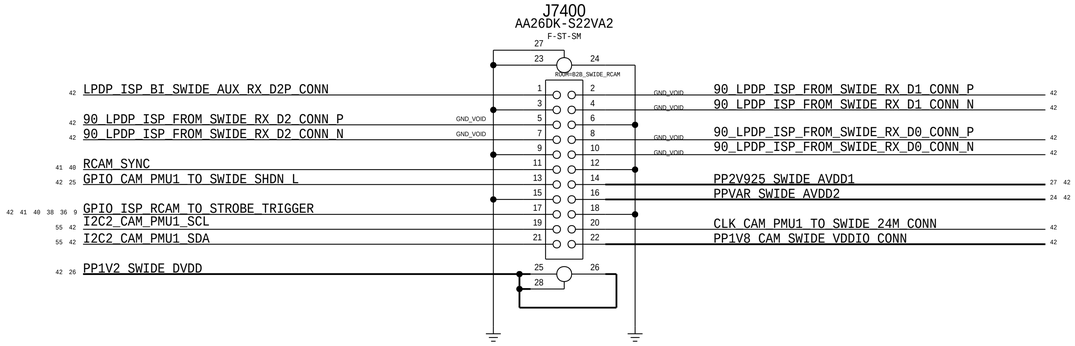


CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHANGED
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*.DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_100UM	P	PWR_100UM	PP1V8_CAM_TELE_VDDIO_CONN	?
PWR_SHAPE	P	PWR_SHAPE	PPVAR_TELE_PVDD_CONN	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHANGED
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*.DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_100UM	S	100UM-249UM_SPACING	PP1V8_CAM_TELE_VDDIO_CONN	?
S_PWR_SHAPE	S	250UM+_SPACING	PPVAR_TELE_PVDD_CONN	?

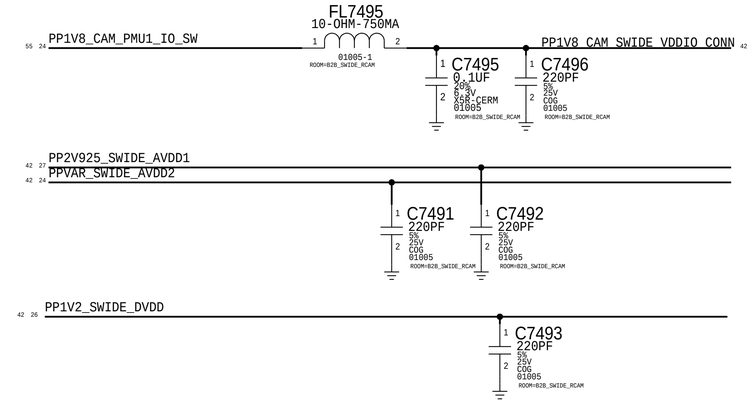
Super Wide Camera Connector

Rcpt: 516S00458 <-- This one on MLB
Plug: 516S00459

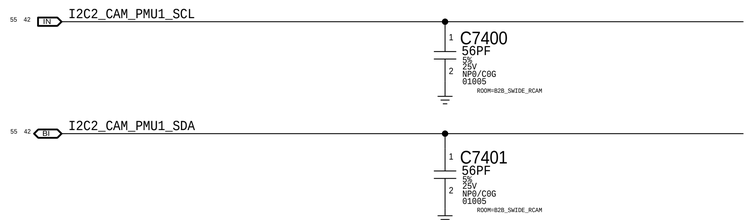


Pin Assignments based on (D42/flex_rcam_mb_l_0.1.0)

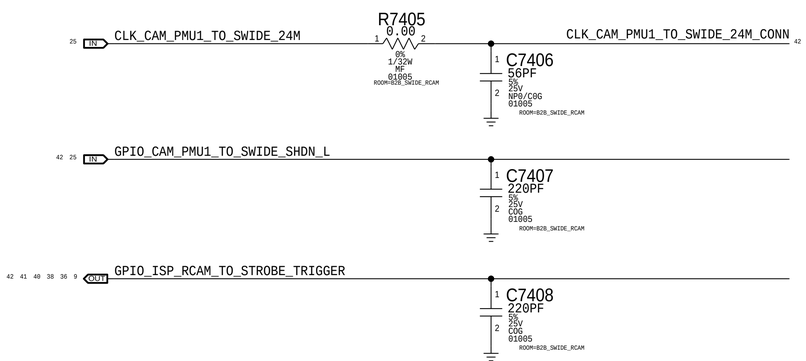
Power Filtering



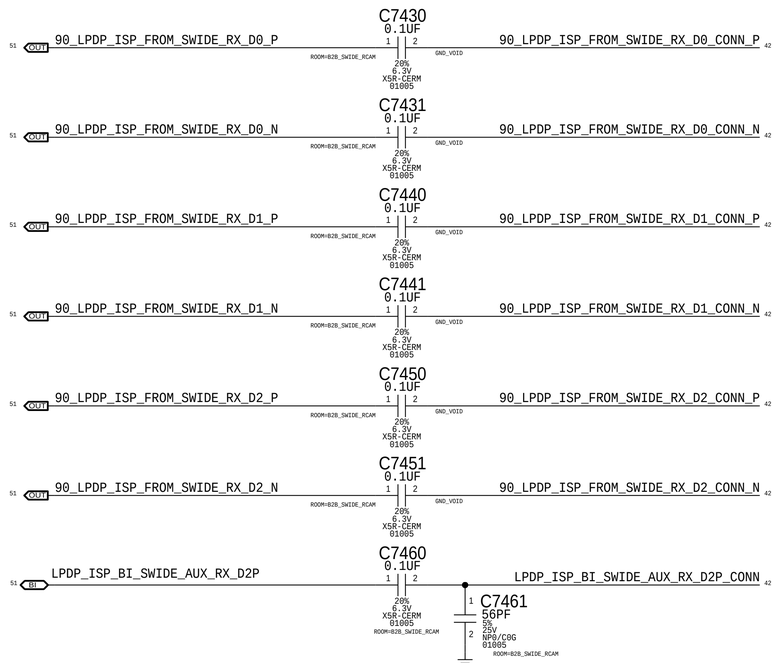
CAM_PMU1 I2C2



IO Filters



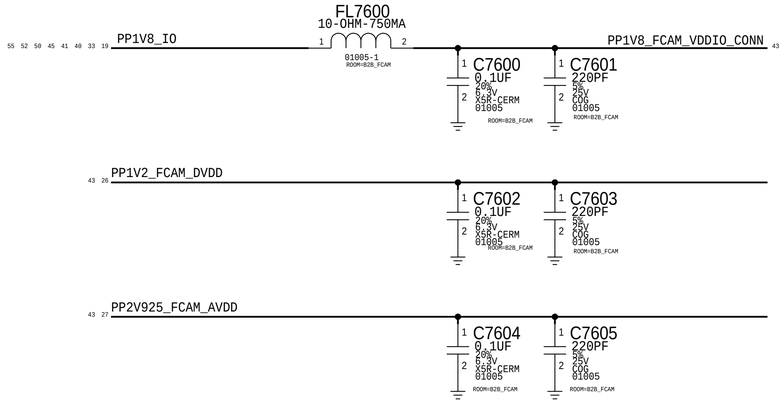
LPDP Filters



CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHECKING
CLASS NAME	PRI	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_100UM	P	PWR_100UM	PP1V8_CAM_SWIDE_VDDIO_CONN	?

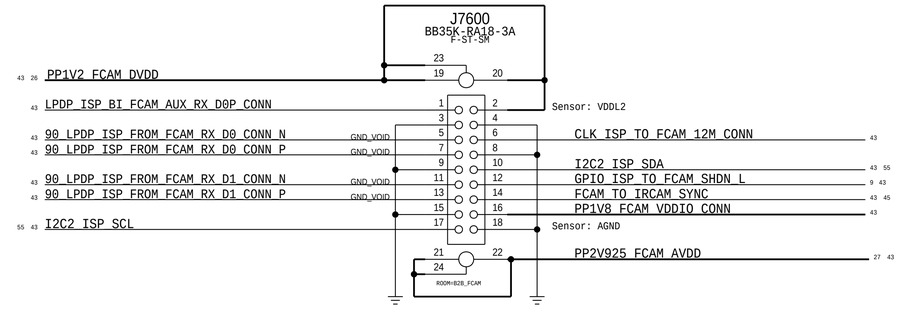
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHECKING
CLASS NAME	PRI	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_100UM	S	100UM-249UM_SPACING	PP1V8_CAM_SWIDE_VDDIO_CONN	?

Power Filtering

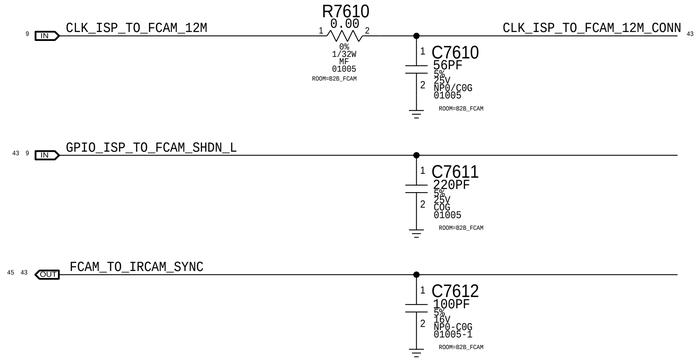


FCAM Connector

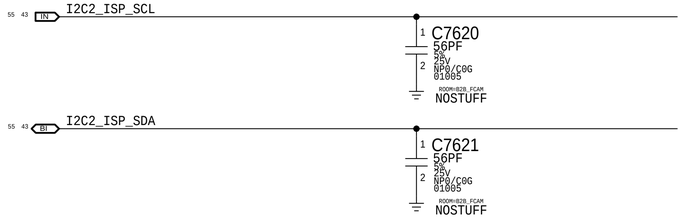
Rcpt: 516S00244 <-- This one on MLB
Plug: 516S00245



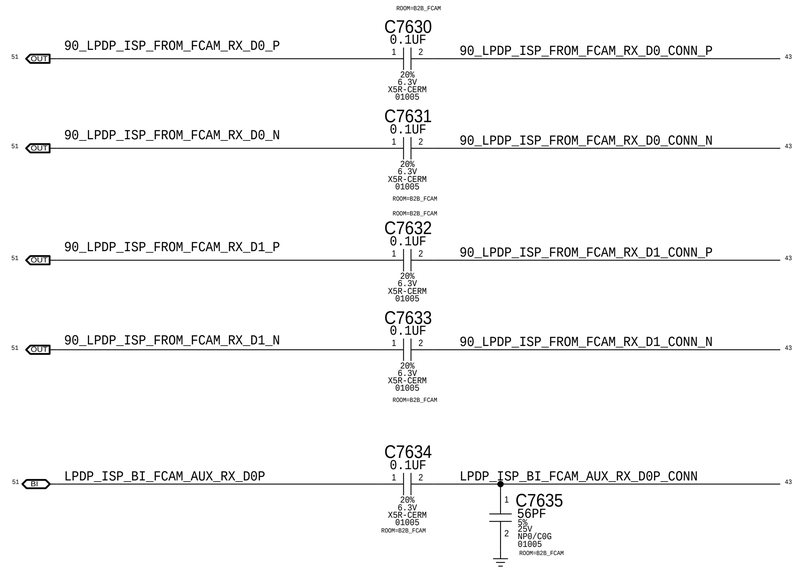
FCAM I/O



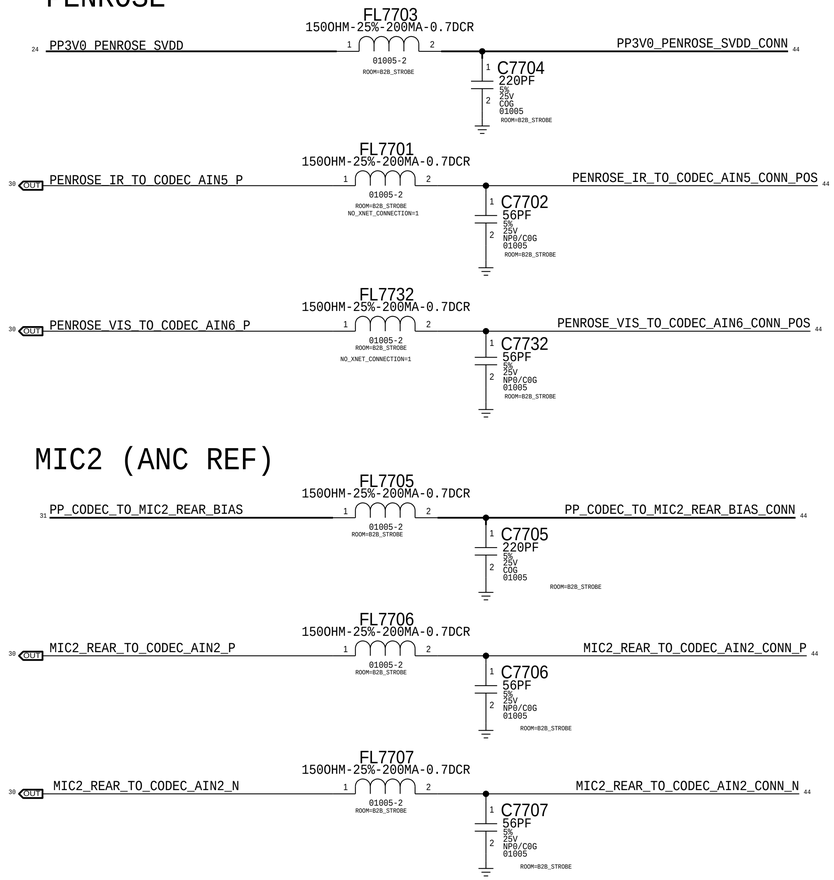
ISP I2C2

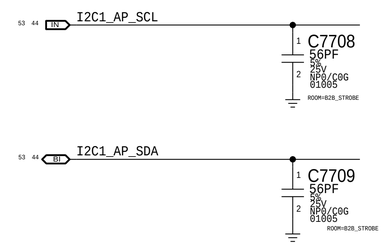


LPDP FILTERS



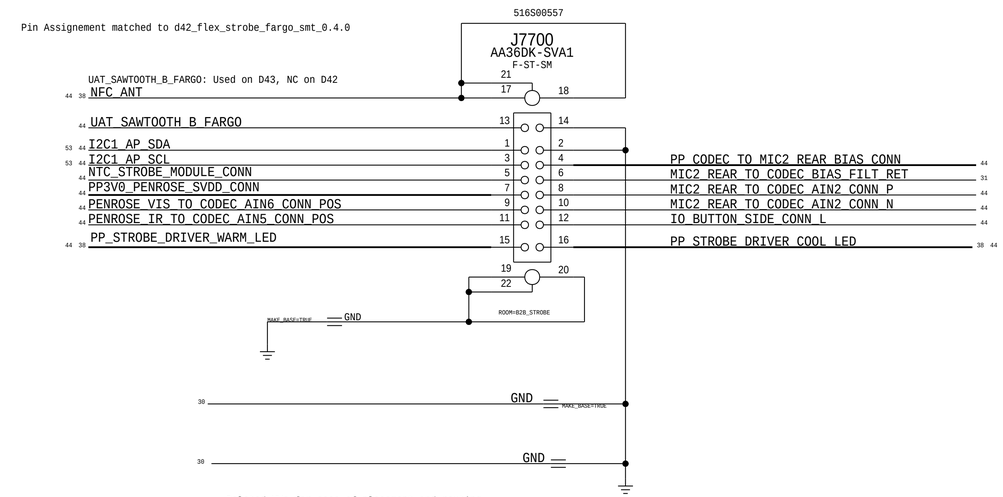
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS CHANGE
CLASS NAME	NET TYPE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_50UM	P	PWR_50UM	PP1V8_FCAM_VDDIO_CONN	?





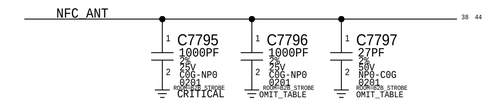
Strobe Connector

Rcpt: 516S00557 <-- This one on MLB
Plug: 516S00558



Deleted XWs for ease of placement and routing

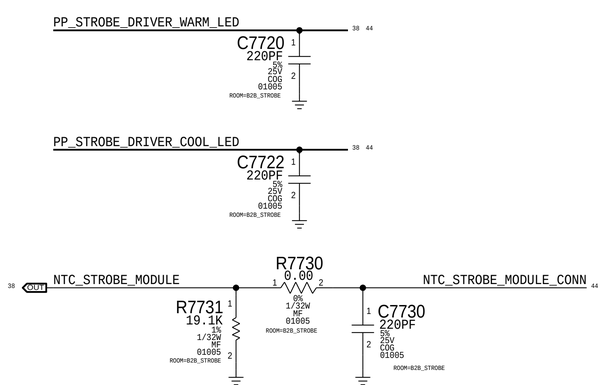
NFC



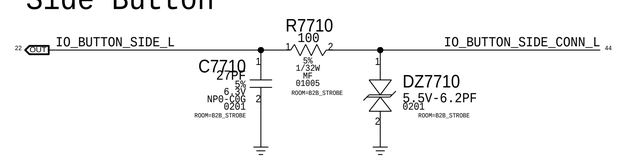
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00011	1	CAP,56pF,50V,01005	C7797	CRITICAL	D421_NFC_MATCH
131S00026	1	CAP,820pF,25V,0201	C7796	CRITICAL	D421_NFC_MATCH

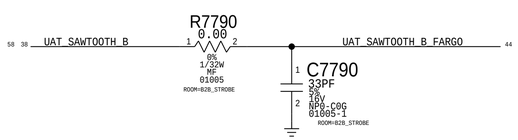
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00116	1	CAP,27pF,50V,01005	C7797	CRITICAL	D431_NFC_MATCH
131S00025	1	CAP,1000pF,25V,0201	C7796	CRITICAL	D431_NFC_MATCH

Strobe Filtering



Side Button

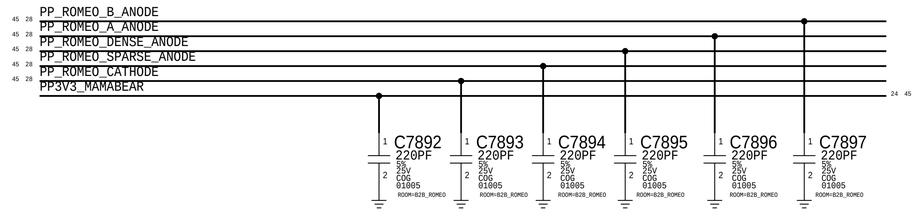




CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	TYPE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_80UM	P	PWR_80UM	PP3V0_PENROSE*	?
PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_DRIVER_WARM_LED,PP_STROBE_DRIVER_COOL_LED	?
PWR_SHAPE	P	PWR_SHAPE	NFC_ANT*	?

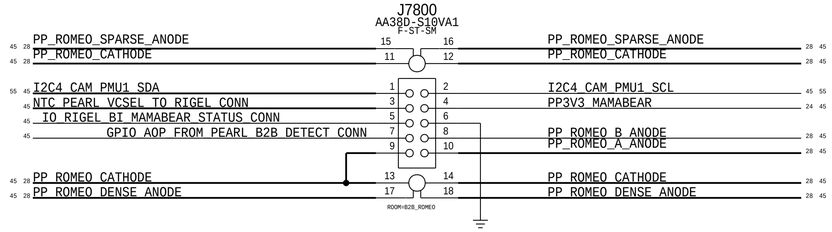
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	TYPE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_SHAPE	S	250UM+_SPACING	PP_STROBE_DRIVER_WARM_LED,PP_STROBE_DRIVER_COOL_LED	?
S_PWR_SHAPE	S	250UM+_SPACING	NFC_ANT*	?

Romeo Power Filtering

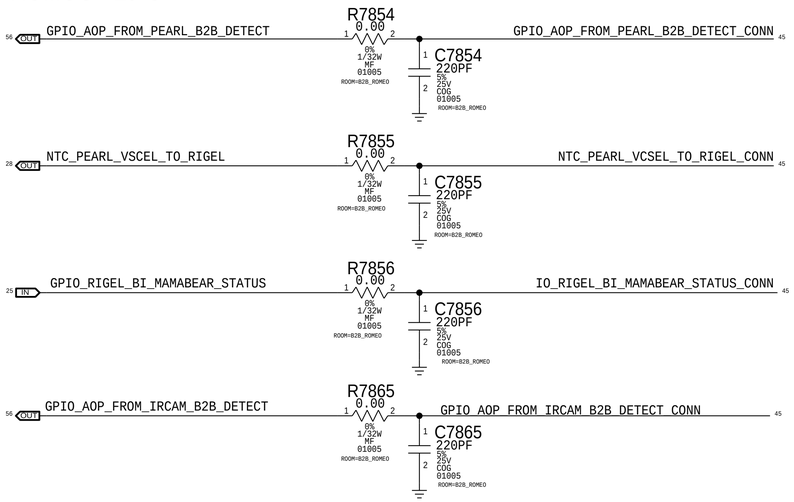


Romeo Connector

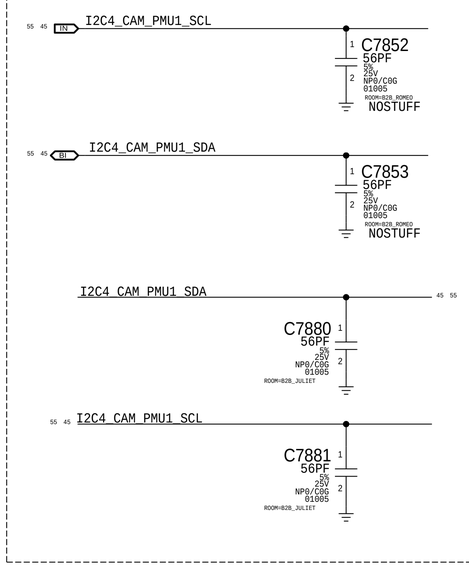
Rcpt: 516S00479 <-- This one on MLB
Plug: 516S00480



Romeo I/O

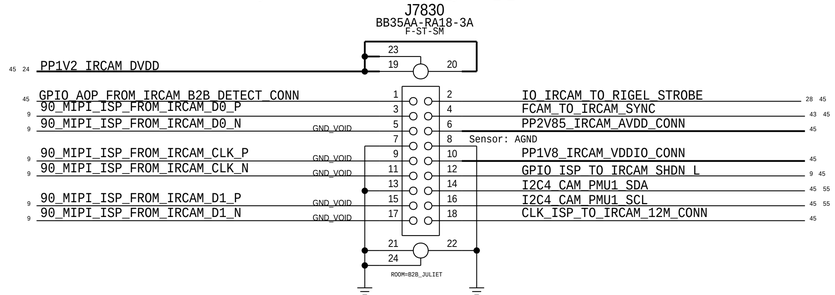


CAM_PMU1 I2C4

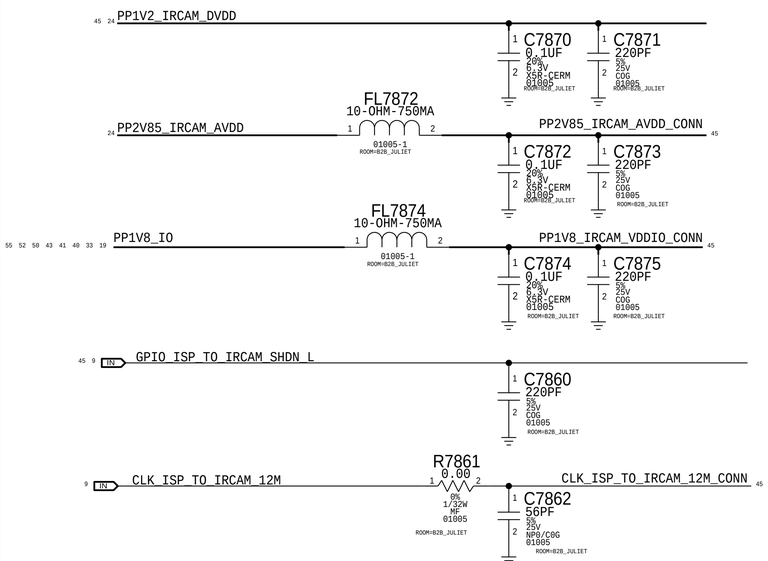


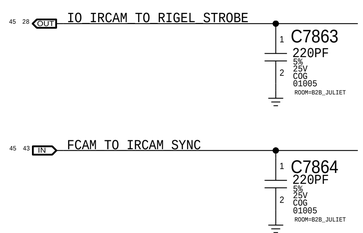
Juliet Connector

Rcpt: 516S00395 <-- This one on MLB
Plug: 516S00396
Pin assignments matched to d42_flex_juliet_l_1.2.0



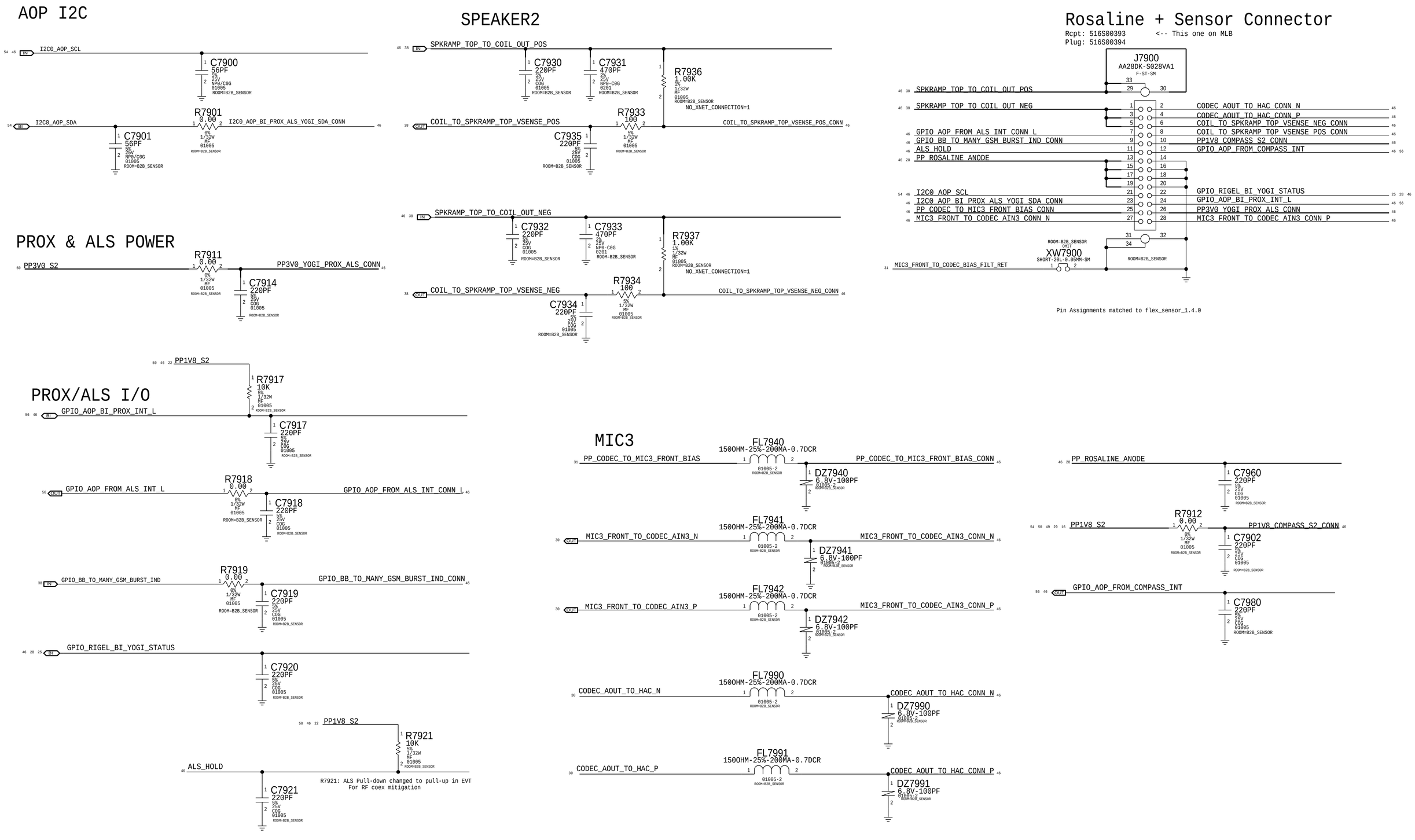
Juliet Power and I/O





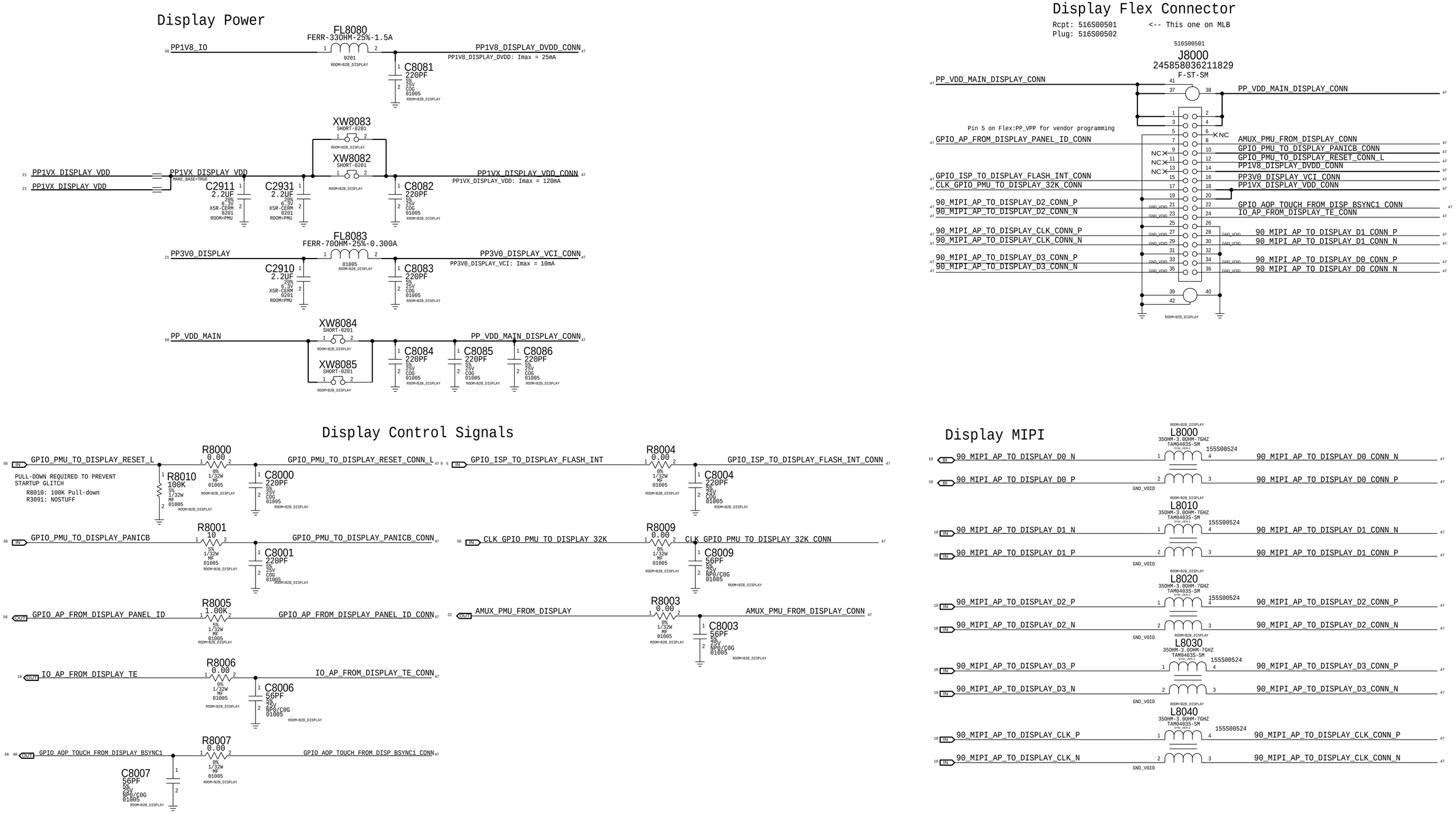
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	...	CONSTRAINT SET		
PWR_100UM	P	PWR_100UM	PP2V85_IRCAM_AVDD_CONN	?
PWR_100UM	P	PWR_100UM	PP_ROMEO_A_ANODE,PP_ROMEO_B_ANODE	?
PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_CATHODE,PP_ROMEO_DENSE_ANODE,PP_ROMEO_SPARSE_ANODE	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	...	CONSTRAINT SET		
S_PWR_100UM	S	100UM-249UM_SPACING	PP_ROMEO_A_ANODE,PP_ROMEO_B_ANODE	?
S_PWR_SHAPE	S	250UM+_SPACING	PP_ROMEO_CATHODE,PP_ROMEO_DENSE_ANODE,PP_ROMEO_SPARSE_ANODE	?



CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	CONST SET	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_80UM	P	PWR_80UM	PP1V8_COMPASS_S2_CONN,PP3V0_YOGI_PROX_ALS_CONN	?
PWR_SHAPE	P	PWR_SHAPE	PP_ROSALINE_ANODE	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	CONST SET	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_SHAPE	S	250UM+_SPACING	PP_ROSALINE_ANODE	?

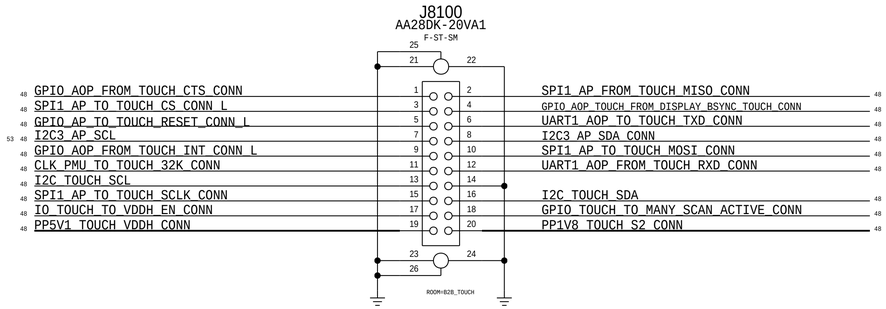


CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	???	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_100UM	P	PWR_100UM	PP1V8_DISPLAY_DVDD_CONN	?
PWR_100UM	P	PWR_100UM	PP3V0_DISPLAY*	?
PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAIN_DISPLAY_CONN,PP1VX_DISPLAY_VDD*	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	???	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_100UM	S	100UM-249UM_SPACING	PP1V8_DISPLAY_DVDD_CONN,PP3V0_DISPLAY*	?
S_PWR_SHAPE	S	250UM+_SPACING	PP_VDD_MAIN_DISPLAY_CONN,PP1VX_DISPLAY_VDD*	?

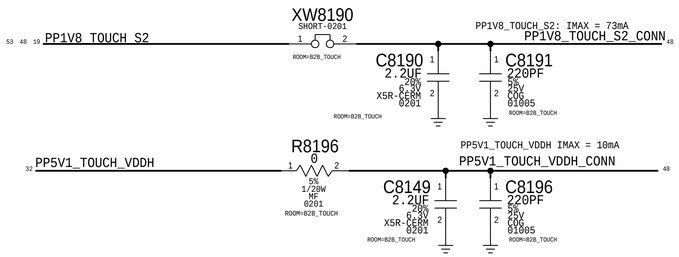
Touch Connector

Rcpt: 516S00515 <-- This one on MLB
Plug: 516S00516

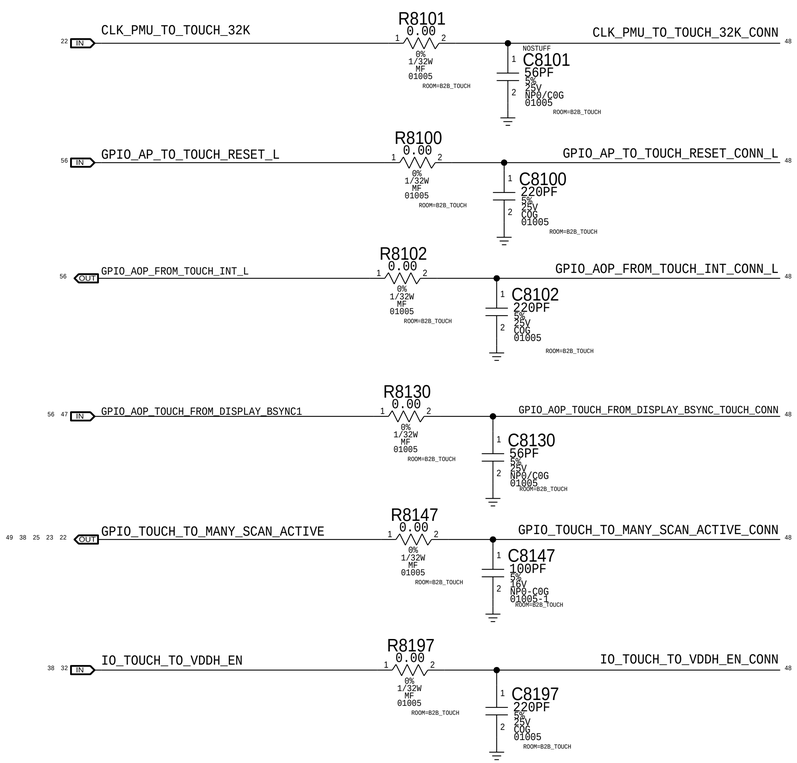


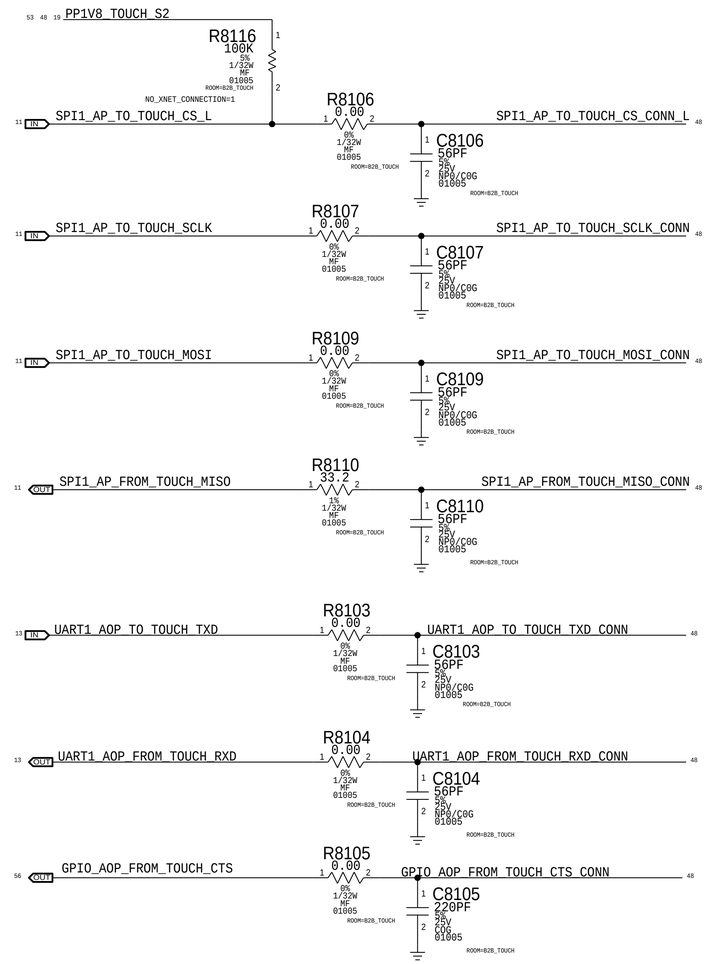
Pin Assignments based on flex_grape_x1372_3.0.0

Touch Power

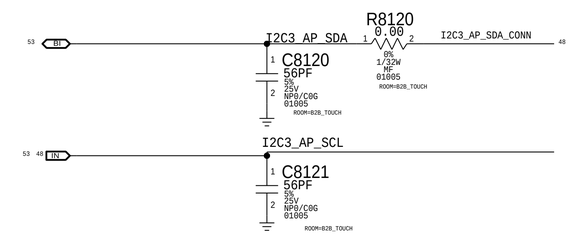


Touch and Misc I/O

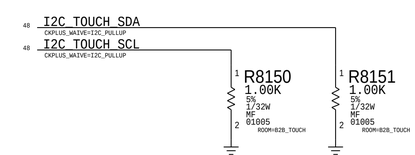




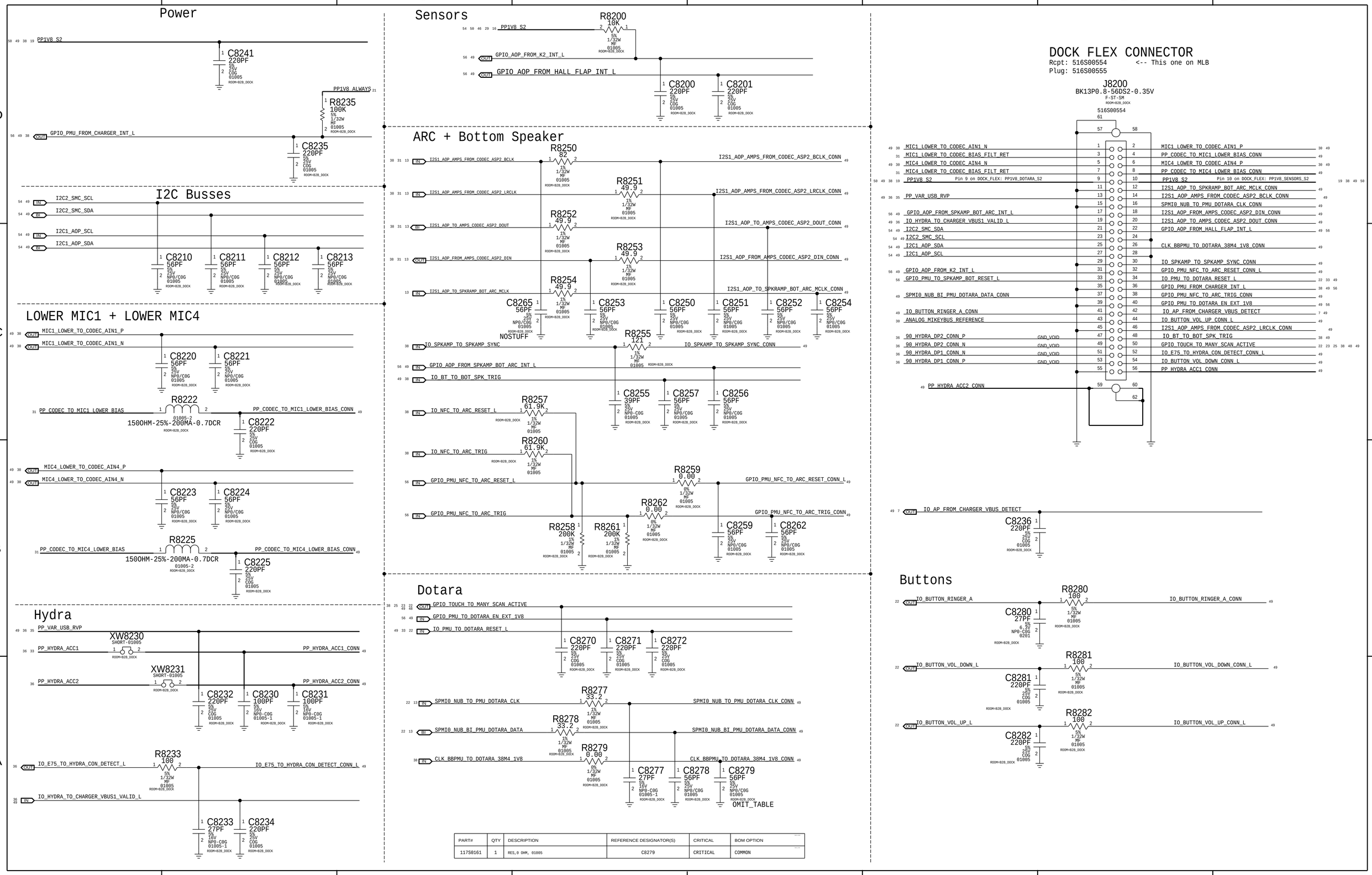
AP I2C Filters



I2C_TOUCH - UNUSED

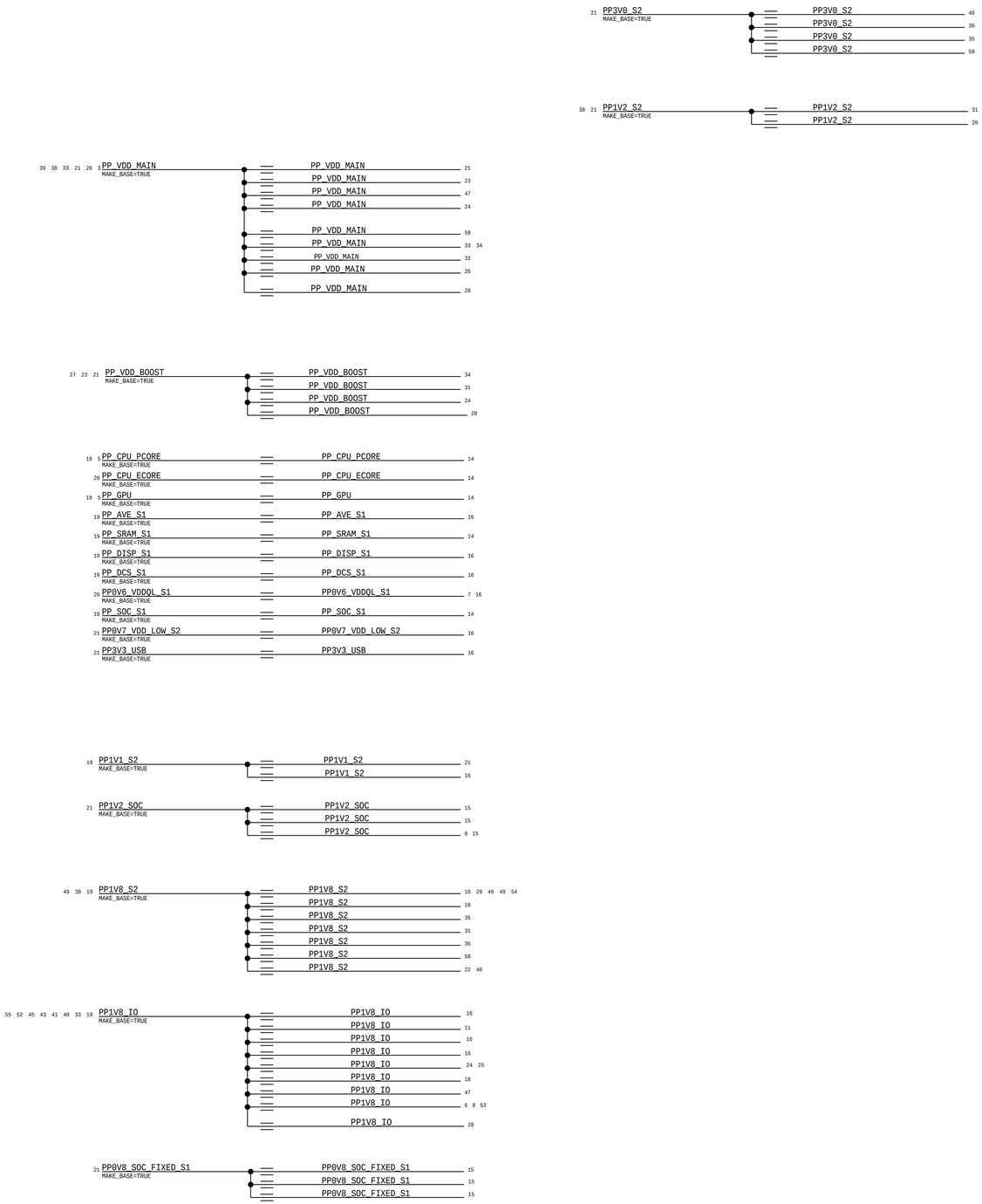


CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_200UM	P	PWR_200UM	PP1V8_TOUCH_S2*	?



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0161	1	RES,0 OHM, 01005	C8279	CRITICAL	COMMON

Medusa Compatibility



ISP: LPDP Lanes

9 OUT	90 LPDP ISP FROM FCAM RX D0 N	MAKE_BASE=TRUE	90 LPDP ISP FROM FCAM RX D0 N	IN 43	
9 OUT	90 LPDP ISP FROM FCAM RX D0 P	MAKE_BASE=TRUE	90 LPDP ISP FROM FCAM RX D0 P	IN 43	Polarity Swapped
9 OUT	90 LPDP ISP FROM FCAM RX D1 N		90 LPDP ISP FROM FCAM RX D1 N	IN 43	
9 OUT	90 LPDP ISP FROM FCAM RX D1 P	MAKE_BASE=TRUE	90 LPDP ISP FROM FCAM RX D1 P	IN 43	Polarity Swapped
9 OUT	90 LPDP ISP FROM WIDE RX D0 P	MAKE_BASE=TRUE	90 LPDP ISP FROM WIDE RX D0 P	IN 40	
9 OUT	90 LPDP ISP FROM WIDE RX D0 N	MAKE_BASE=TRUE	90 LPDP ISP FROM WIDE RX D0 N	IN 40	
9 OUT	90 LPDP ISP FROM WIDE RX D2 P	MAKE_BASE=TRUE	90 LPDP ISP FROM WIDE RX D2 P	IN 40	
9 OUT	90 LPDP ISP FROM WIDE RX D2 N	MAKE_BASE=TRUE	90 LPDP ISP FROM WIDE RX D2 N	IN 40	
9 OUT	90 LPDP ISP FROM WIDE RX D1 N	MAKE_BASE=TRUE	90 LPDP ISP FROM WIDE RX D1 N	IN 40	Polarity Swapped
9 OUT	90 LPDP ISP FROM WIDE RX D1 P	MAKE_BASE=TRUE	90 LPDP ISP FROM WIDE RX D1 P	IN 40	
9 OUT	90 LPDP ISP FROM SWIDE RX D2 N	MAKE_BASE=TRUE	90_LPDP_ISP_FROM_SWIDE_RX_D2_N	IN 42	
9 OUT	90 LPDP ISP FROM SWIDE RX D2 P	MAKE_BASE=TRUE	90 LPDP ISP FROM SWIDE RX D2 P	IN 42	Polarity Swapped
9 OUT	90 LPDP ISP FROM SWIDE RX D1 N	MAKE_BASE=TRUE	90 LPDP ISP FROM SWIDE RX D1 N	IN 42	
9 OUT	90 LPDP ISP FROM SWIDE RX D1 P	MAKE_BASE=TRUE	90 LPDP ISP FROM SWIDE RX D1 P	IN 42	Polarity Swapped
9 OUT	90 LPDP ISP FROM SWIDE RX D0 N	MAKE_BASE=TRUE	90_LPDP_ISP_FROM_SWIDE_RX_D0_N	IN 42	
9 OUT	90 LPDP ISP FROM SWIDE RX D0 P	MAKE_BASE=TRUE	90 LPDP ISP FROM SWIDE RX D0 P	IN 42	Polarity Swapped
9 OUT	NC_LPDP_ISP_RX_D8_P	MAKE_BASE=TRUE	NO_TEST=1 NC_LPDP_ISP_RX_D8_P		
9 OUT	NC_LPDP_ISP_RX_D8_N	MAKE_BASE=TRUE	NO_TEST=1 NC_LPDP_ISP_RX_D8_N		
9 OUT	90 LPDP ISP FROM TELE RX D1 P	MAKE_BASE=TRUE	90 LPDP ISP FROM TELE RX D1 P	IN 41	
9 OUT	90 LPDP ISP FROM TELE RX D1 N	MAKE_BASE=TRUE	90 LPDP ISP FROM TELE RX D1 N	IN 41	
9 OUT	90 LPDP ISP FROM TELE RX D0 N		90_LPDP_ISP_FROM_TELE_RX_D0_N	IN 41	Polarity Swapped
9 OUT	90 LPDP ISP FROM TELE RX D0 P	MAKE_BASE=TRUE	90 LPDP ISP FROM TELE RX D0 P	IN 41	
9 OUT	90 LPDP ISP FROM TELE RX D2 P	MAKE_BASE=TRUE	90 LPDP ISP FROM TELE RX D2 P	IN 41	
9 OUT	90 LPDP ISP FROM TELE RX D2 N	MAKE_BASE=TRUE	90 LPDP ISP FROM TELE RX D2 N	IN 41	

ISP: LPDP Aux

9 BI	LPDP_ISP_BI_FCAM_AUX_RX_D0P	MAKE_BASE=TRUE	LPDP_ISP_BI_FCAM_AUX_RX_D0P	BI 43
9 BI	LPDP_ISP_BI_SWIDE_AUX_RX_D2P	MAKE_BASE=TRUE	LPDP_ISP_BI_SWIDE_AUX_RX_D2P	BI 42
9 BI	LPDP_ISP_BI_TELE_AUX_RX_D5P	MAKE_BASE=TRUE	LPDP_ISP_BI_TELE_AUX_RX_D5P	BI 41
9 BI	LPDP_ISP_BI_WIDE_AUX_RX_D9P	MAKE_BASE=TRUE	LPDP_ISP_BI_WIDE_AUX_RX_D9P	BI 40

Mt. Whitney vs Avus

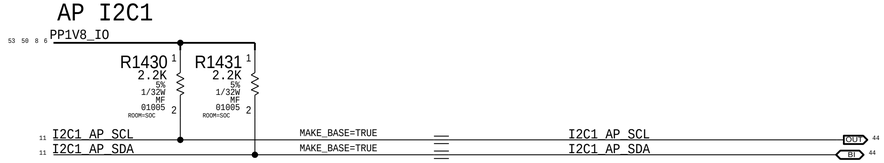
56 PP1V8_IO ═══ PP1V8_IO 19 33 40 41 43 45 50 55
MAKE_BASE=TRUE

AP_GPIO19: PMU ID
WHITNEY: AP_GPIO_19 = NC
AVUS: AP_GPIO_19 = PP1V8_IO

AP I2C

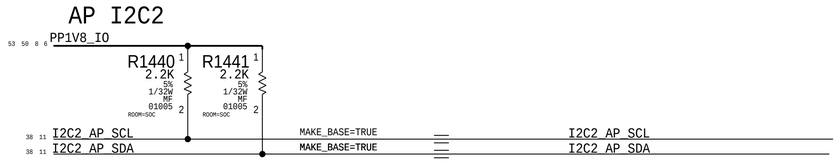
AP I2C0

AP I2C1



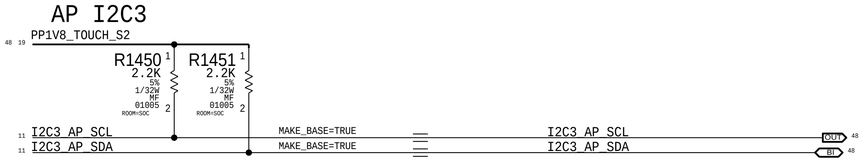
MASTER	AP	NUMBER	I2C1	DIAGS NUMBER	1	SPEED	100KHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
MIC2	PP1V8_IO		0x56	0xAC, 0xAD	1MHz		STROBE_FLEX

AP I2C2



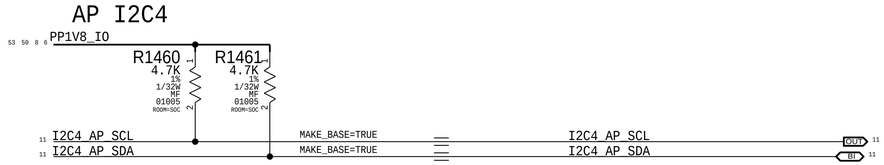
MASTER	AP	NUMBER	I2C2	DIAGS NUMBER	2	SPEED	1MHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
TOP SPK AMP	PP1V8_IO		0x40	0x80, 0x81	1MHz		MLB_BOT

AP I2C3



MASTER	AP	NUMBER	I2C3	DIAGS NUMBER	3	SPEED	400KHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
ROSWELL	PP1V8_TOUCH_S2		0x10	0x20, 0x21	1MHz		TOUCH_FLEX
TOUCH EEPROM	PP1V8_TOUCH_S2		0x51	0xA2, 0xA3	1MHz		TOUCH_FLEX

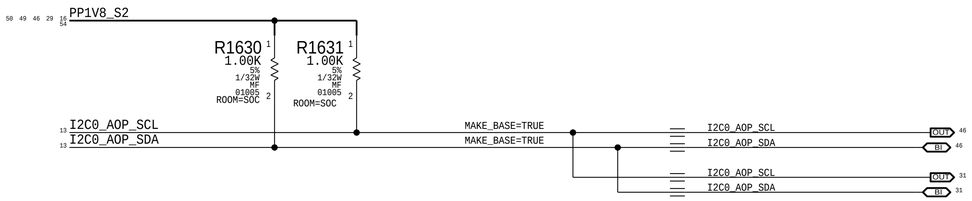
AP I2C4



MASTER	AP	NUMBER	I2C4	DIAGS NUMBER	4	SPEED	400KHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
LYNX	PP1V8_IO		0x71	0xE2	TBD		MLB_TOP

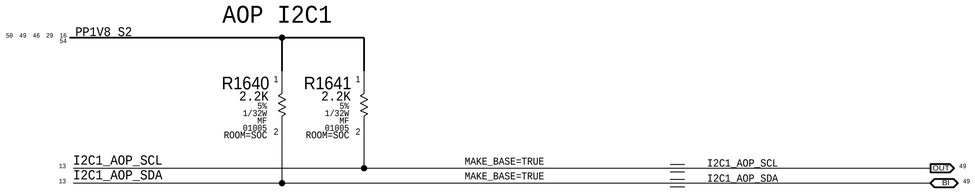
AOP/SMC I2C

AOP I2C0



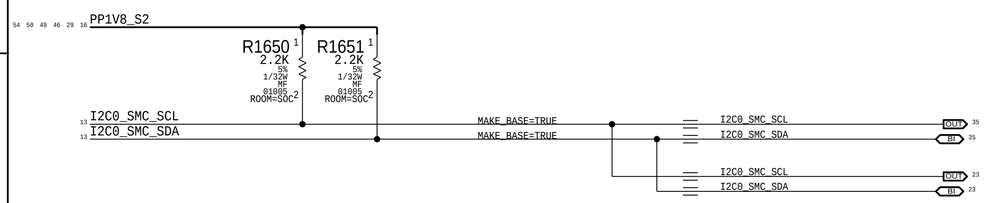
MASTER	AOP	NUMBER	I2C0	DIAGS NUMBER	5	SPEED	750KHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
DOPPLER	PP1V8_S2		0x58	0xB0, 0xB1	1MHZ		SENSOR_FLEX
FOXHOUND	PP1V8_S2		0x29	0x52, 0x53	1MHZ		SENSOR_FLEX
YOGI	PP1V8_S2		0x33	0x66, 0x67	1MHZ		SENSOR_FLEX
MOLY	PP1V8_S2		0x0E	0x1C, 0x1D	1MHZ		SENSOR_FLEX
BRIGHTON	PP1V8_S2		0x4A	0x94, 0x95	TBD		MLB_TOP

AOP I2C1



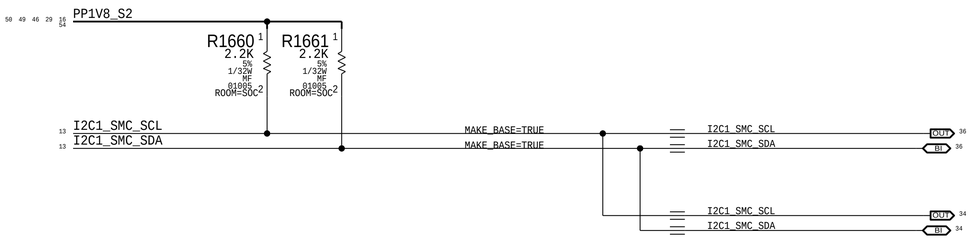
MASTER	AOP	NUMBER	I2C1	DIAGS NUMBER	6	SPEED	400KHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
ARC AMP	PP1V8_S2		0x41	0x82, 0x83	1MHZ		SOUTH_HUB
BOTTOM SPKR	PP1V8_S2		0x40	0x80, 0x81	1MHZ		SOUTH_HUB
K2	PP1V8_S2		0x5C	0xB8, 0xB9	400KHZ		DOCK_FLEX
SAKONNET	PP1V8_S2		0x08	0x10, 0x11	400KHZ		ARC_FLEX

SMC I2C0



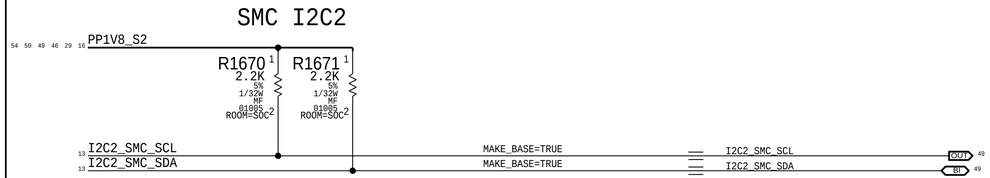
MASTER	SMC	NUMBER	I2C0	DIAGS NUMBER	7	SPEED	400KHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
CCG2	PP1V8_S2		0x12	0x24, 0x25	1MHz		MLB_TOP
BOOST	PP1V8_S2		0x75	0xEA, 0xEB	400KHZ		MLB_TOP

SMC I2C1

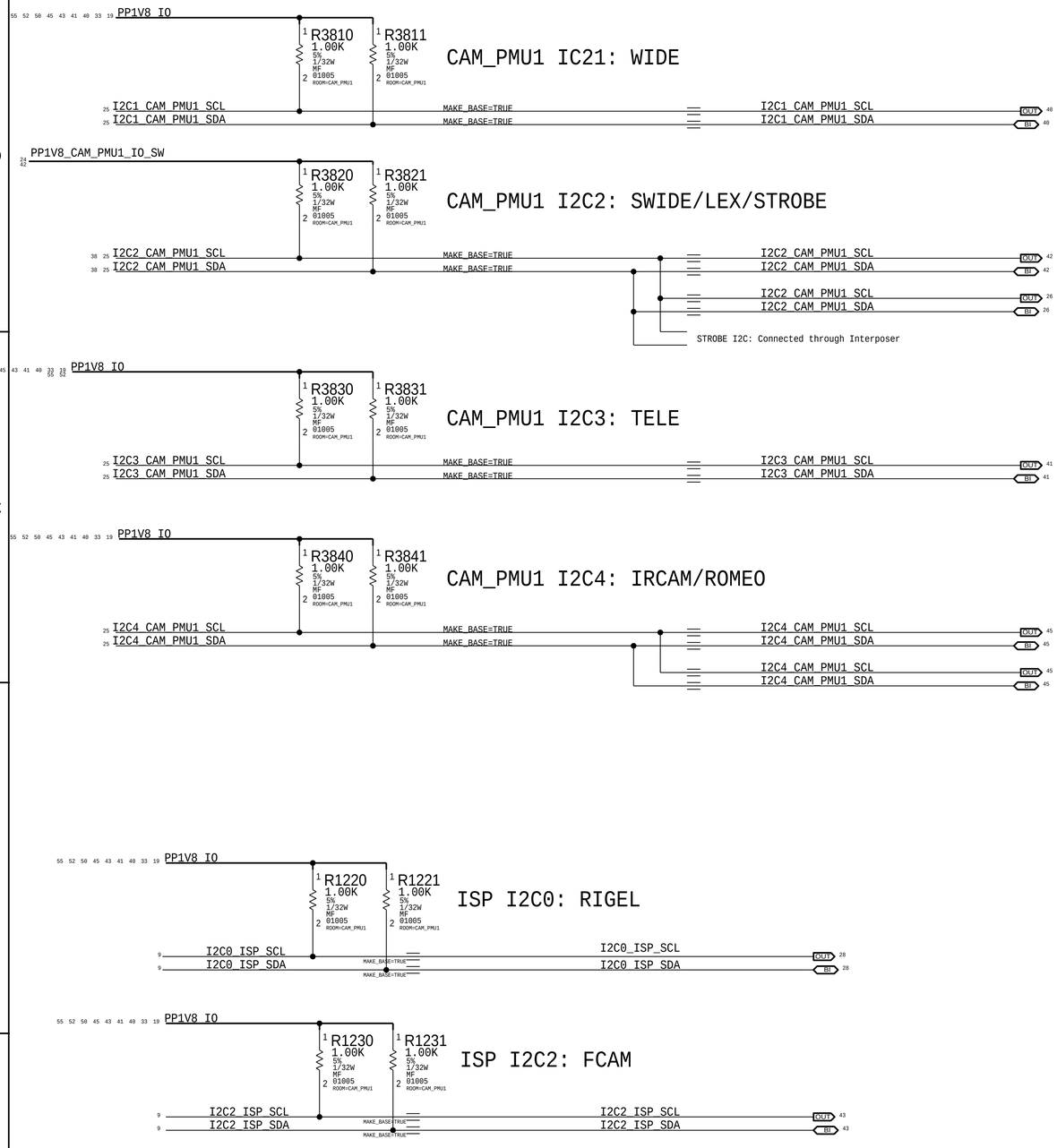


MASTER	SMC	NUMBER	I2C1	DIAGS NUMBER	8	SPEED	400KHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
HYDRA	PP1V8_S2		0x1A	0x34, 0x35	400KHZ		MLB_TOP
GECKO	PP1V8_S2		0x52	0xA4, 0XA5	1MHZ		MLB_TOP

SMC I2C2



MASTER	SMC	NUMBER	I2C2	DIAGS NUMBER	9	SPEED	400KHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
YANGTZE	PP1V8_S2		0x71	0xE2, 0xE3	400KHZ		SOUTH_HUB
VERIDIAN	PP1V8_S2		0x0B	0x16, 0X17	1MHZ		BMU_FLEX



MASTER	CAMERA_PMU	NUMBER	I2C1	DIAGS NUMBER	TBD	SPEED	1MHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
TORONTO (ON)	PP1V8_IO		0x10	0x20, 0x21	1MHz		WIDE_CAM
RAMAN	PP1V8_IO		0x3C	0x78, 0x79	1MHZ		WIDE_CAM

MASTER	CAMERA_PMU	NUMBER	I2C2	DIAGS NUMBER	TBD	SPEED	1MHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
WINNIPEG (MB)	PP1V8_IO_SW		0x20	0x40, 0x41	1MHz		SWIDE_CAM
LEX	PP1V8_IO_SW		0x75	0xEA, 0xEB	1MHZ		MLB_TOP
STROBE	PP1V8_IO_SW		0x65	0xCA, 0xCB	1MHZ		MLB_BOT

MASTER	CAMERA_PMU	NUMBER	I2C3	DIAGS NUMBER	TBD	SPEED	1MHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
BILLINGS+ (AB)	PP1V8_IO		0x20	0x40, 0x41	1MHz		TELE_CAM
RAMAN	PP1V8_IO		0x1C	0x38, 0x39	1MHZ		TELE_CAM

MASTER	CAMERA_PMU	NUMBER	I2C4	DIAGS NUMBER	TBD	SPEED	1MHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
JULIET	PP1V8_IO		0x18	0x30, 0x31	1MHz		MLB_TOP
ROMEO	PP1V8_IO		0x66	0xCC, 0xCD	1MHZ		MLB_TOP

MASTER	ISP	NUMBER	I2C0	DIAGS NUMBER	TBD	SPEED	1MHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
RIGEL	PP1V8_IO		0x55	0xAA, 0xAB	1MHz		MLB_TOP

MASTER	ISP	NUMBER	I2C1	DIAGS NUMBER	TBD	SPEED	1MHZ
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED		LOCATION
POTOMAC (MD)	PP1V8_IO		0x10	0x20, 0x21	1MHz		FCAM

AOP

SCM_SPI TRIGGER & CS >

SCM_I2CM0 TRIGGER --->

SCM_I2CM1 TRIGGER >

AOP_FUNC_0	13	GPIO_AOP_FROM_IMU_DATARDY	GPIO AOP FROM IMU DATARDY	MAKE_BASE=TRUE	IN	5 29
AOP_FUNC_1	13	GPIO_AOP_TO_IMU_SPI_CS_L	GPIO AOP TO IMU SPI CS L	MAKE_BASE=TRUE	OUT	29
AOP_FUNC_2	13	GPIO_AOP_FROM_PEARL_B2B_DETECT	GPIO AOP FROM PEARL B2B DETECT	MAKE_BASE=TRUE	IN	45
AOP_FUNC_3	13	GPIO_AOP_TO_R1_SPI_CS_L	GPIO AOP TO R1 SPI CS L	MAKE_BASE=TRUE	IN	58
AOP_FUNC_4	13	GPIO_AOP_FROM_R1_INT	GPIO AOP FROM R1 INT	MAKE_BASE=TRUE	IN	58
AOP_FUNC_5	13	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	GPIO AOP TO R1 COREDUMP TRIGGER	MAKE_BASE=TRUE	OUT	58
AOP_FUNC_6	13	GPIO_AOP_TO_R1_TIME_SYNC	GPIO AOP TO R1 TIME SYNC	MAKE_BASE=TRUE	OUT	58
AOP_FUNC_7	13	GPIO_AOP_TO_CODEC_RESET_L	GPIO AOP TO CODEC RESET L	MAKE_BASE=TRUE	OUT	5 31
AOP_FUNC_8	13	GPIO_AOP_TO_CODEC_CLP_EN	GPIO AOP TO CODEC CLP EN	MAKE_BASE=TRUE	OUT	5 31
AOP_FUNC_9	13	GPIO_AOP_FROM_IRCAM_B2B_DETECT	GPIO AOP FROM IRCAM B2B DETECT	MAKE_BASE=TRUE	IN	45
AOP_FUNC_10	13	GPIO_AOP_FROM_NFC_HOST_WAKE	GPIO AOP FROM NFC HOST WAKE	MAKE_BASE=TRUE	IN	38
AOP_FUNC_11	13	GPIO_AOP_FROM_SPKAMP_BOT_ARC_INT_L	GPIO AOP FROM SPKAMP BOT ARC INT L	MAKE_BASE=TRUE	IN	49
AOP_FUNC_12	13	GPIO_AOP_TO_WLAN_CONTEXT_A	GPIO AOP TO WLAN CONTEXT A	MAKE_BASE=TRUE	OUT	38
AOP_FUNC_13	13	GPIO_AOP_TO_WLAN_CONTEXT_B	GPIO AOP TO WLAN CONTEXT B	MAKE_BASE=TRUE	OUT	38
AOP_FUNC_14	13	GPIO_AOP_FROM_TOUCH_CTS	GPIO AOP FROM TOUCH CTS	MAKE_BASE=TRUE	IN	48
AOP_FUNC_15	13	GPIO_AOP_BI_PROX_INT_L	GPIO AOP BI PROX INT L	MAKE_BASE=TRUE	IN	46
AOP_FUNC_16	13	GPIO_AOP_FROM_ALS_INT_L	GPIO AOP FROM ALS INT L	MAKE_BASE=TRUE	IN	46
AOP_FUNC_17	13	GPIO_AOP_FROM_K2_INT_L	GPIO AOP FROM K2 INT L	MAKE_BASE=TRUE	IN	49
AOP_FUNC_18	13	GPIO_AOP_FROM_COMPASS_INT	GPIO AOP FROM COMPASS INT	MAKE_BASE=TRUE	IN	46
AOP_FUNC_19	13	GPIO_AOP_FROM_HALL_CASE_INT_L	GPIO AOP FROM HALL CASE INT L	MAKE_BASE=TRUE	IN	38
AOP_FUNC_20	13	GPIO_AOP_FROM_HALL_FLAP_INT_L	GPIO AOP FROM HALL FLAP INT L	MAKE_BASE=TRUE	IN	49
AOP_FUNC_21	13	GPIO_AOP_FROM_TOUCH_INT_L	GPIO AOP FROM TOUCH INT L	MAKE_BASE=TRUE	IN	48
AOP_FUNC_22	13	GPIO_AOP_TOUCH_FROM_DISPLAY_BSYNC1	GPIO AOP TOUCH FROM DISPLAY BSYNC1	MAKE_BASE=TRUE	IN	47 48

PMU

HOLD Bit: Held Through 1 Reset

HOLD Bit: Held Through 1 Reset

HOLD Bit: Held Through 1 Reset

HOLD Bit: Held Through 1 Reset

Sequenced GPIOs

	GPIO_1	22	GPIO_PMU_TO_CCG2_RESET_L	GPIO PMU TO CCG2 RESET L	MAKE_BASE=TRUE	OUT	35
	GPIO_2	22	NC_PMU_GPIO_2	NC PMU GPIO 2	MAKE_BASE=TRUE NO_TEST=1		
PMU_SWDIO	GPIO_3	22	SWD_NUB_BI_PMU_SWDIO	SWD NUB BI PMU SWDIO	MAKE_BASE=TRUE	OUT	5 13
	GPIO_4	22	GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO PMU FROM WLAN HOST WAKE	MAKE_BASE=TRUE	IN	38
	GPIO_5	22	GPIO_PMU_NFC_TO_ARC_TRIG	GPIO PMU NFC TO ARC TRIG	MAKE_BASE=TRUE	OUT	49
	GPIO_6	22	GPIO_PMU_NFC_TO_ARC_RESET_L	GPIO PMU NFC TO ARC RESET L	MAKE_BASE=TRUE	OUT	49
	GPIO_7	22	NC_PMU_GPIO_7	NC PMU GPIO 7	MAKE_BASE=TRUE NO_TEST=1		
	GPIO_8	22	NC_PMU_GPIO_8	NC PMU GPIO 8	MAKE_BASE=TRUE NO_TEST=1		
	GPIO_9	22	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L	GPIO PMU FROM BB PCIE HOST WAKE 1V2 L	MAKE_BASE=TRUE	IN	38
	GPIO_10	22	NC_PMU_GPIO_10	NC PMU GPIO 10	MAKE_BASE=TRUE NO_TEST=1		
	GPIO_11	22	GPIO_PMU_FROM_CHARGER_INT_L	GPIO PMU FROM CHARGER INT L	MAKE_BASE=TRUE	IN	38 49
	GPIO_12	22	GPIO_PMU_FROM_CODEC_WAKE_L	GPIO PMU FROM CODEC WAKE L	MAKE_BASE=TRUE	IN	31
	GPIO_13	22	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	GPIO PMU TO AMUX PMU SUPER TP	MAKE_BASE=TRUE CKPLUS_WAIVE=SINGLE_COMP_NET	OUT	22
	GPIO_14	22	GPIO_PMU_TO_R1_RESET_L	GPIO PMU TO R1 RESET L	MAKE_BASE=TRUE	OUT	58
	GPIO_15	22	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	GPIO PMU TO NAND LOW BATT BOOT L	MAKE_BASE=TRUE	OUT	18
IRQ	GPIO_16	22	CLK_GPIO_PMU_TO_DISPLAY_32K	CLK GPIO PMU TO DISPLAY 32K	MAKE_BASE=TRUE	OUT	47
	GPIO_17	22	GPIO_PMU_TO_WLAN_REG_ON	GPIO PMU TO WLAN REG ON	MAKE_BASE=TRUE	OUT	38
	GPIO_18	22	CLK_GPIO_PMU_TO_WLAN_R1_32K	CLK GPIO PMU TO WLAN R1 32K	MAKE_BASE=TRUE	OUT	22 38 58
	GPIO_19	22	GPIO_PMU_TO_SPKAMP_BOT_RESET_L	GPIO PMU TO SPKAMP BOT RESET L	MAKE_BASE=TRUE	OUT	49
	GPIO_20	22	GPIO_PMU_TO_DOTARA_EN_EXT_1V8	GPIO PMU TO DOTARA EN EXT 1V8	MAKE_BASE=TRUE	OUT	49
	GPIO_21	22	GPIO_PMU_TO_BBPMU_RESET_L	GPIO PMU TO BBPMU RESET L	MAKE_BASE=TRUE	OUT	38
	GPIO_22	22	GPIO_PMU_TO_NFC_EN	GPIO PMU TO NFC EN	MAKE_BASE=TRUE	OUT	38
	GPIO_23	22	GPIO_PMU_TO_BOOST_EN	GPIO PMU TO BOOST EN	MAKE_BASE=TRUE	OUT	23
	GPIO_24	22	GPIO_PMU_TO_DISPLAY_PANICB	GPIO PMU TO DISPLAY PANICB	MAKE_BASE=TRUE	OUT	47
	GPIO_25	22	GPIO_PMU_TO_DISPLAY_RESET_L	GPIO PMU TO DISPLAY RESET L	MAKE_BASE=TRUE	OUT	47

GPIO_PMU_TO_WLAN_REG_ON: HOLD bit required

CLK_GPIO_PMU_TO_WLAN_R1_32K: HOLD bit required

SOC

1.2V

NC_AP_GPIO[0-1]: Placeholder Great Dane [Dev]

GPIO_0	12	NC_AP_GPIO0	NC AP GPIO0	MAKE_BASE=TRUE NO_TEST=1		
GPIO_1	12	NC_AP_GPIO1	NC AP GPIO1	MAKE_BASE=TRUE NO_TEST=1		
GPIO_2	12	NC_AP_GPIO2	NC AP GPIO2	MAKE_BASE=TRUE NO_TEST=1		
GPIO_3	12	GPIO_AP_FROM_WLAN_TIME_SYNC_1V2	GPIO AP FROM WLAN TIME SYNC 1V2	MAKE_BASE=TRUE	IN	38
GPIO_4	12	GPIO_AP_TO_BB_COREDUMP_1V2	GPIO AP TO BB COREDUMP 1V2	MAKE_BASE=TRUE	IN	38
GPIO_5	12	GPIO_AP_FROM_BB_RESET_DETECT_1V2_L	GPIO AP FROM BB RESET DETECT 1V2 L	MAKE_BASE=TRUE		38
GPIO_6	12	NC_AP_GPIO6	NC AP GPIO6	MAKE_BASE=TRUE NO_TEST=1		
GPIO_7	12	NC_AP_GPIO7	NC AP GPIO7	MAKE_BASE=TRUE NO_TEST=1		
GPIO_8	12	NC_AP_GPIO8	NC AP GPIO8	MAKE_BASE=TRUE NO_TEST=1		
GPIO_9	12	GPIO_BOARD_REV3	GPIO BOARD REV3	MAKE_BASE=TRUE	IN	6
GPIO_10	12	GPIO_BOARD_REV2	GPIO BOARD REV2	MAKE_BASE=TRUE	IN	6
GPIO_11	12	GPIO_BOARD_REV1	GPIO BOARD REV1	MAKE_BASE=TRUE	IN	6
GPIO_12	12	GPIO_BOARD_REV0	GPIO BOARD REV0	MAKE_BASE=TRUE	IN	6
GPIO_13	12	GPIO_AP_CANARY1	GPIO AP CANARY1	MAKE_BASE=TRUE	IN	38
GPIO_14	12	GPIO_AP_CANARY2	GPIO AP CANARY2	MAKE_BASE=TRUE	IN	38
GPIO_15	12	GPIO_AP_BI_CCG2_SWDIO	GPIO AP BI CCG2 SWDIO	MAKE_BASE=TRUE	BI	35
GPIO_16	12	GPIO_AP_TO_CCG2_SWCLK	GPIO AP TO CCG2 SWCLK	MAKE_BASE=TRUE	OUT	5 35
GPIO_17	12	NC_AP_GPIO17	NC AP GPIO17	MAKE_BASE=TRUE NO_TEST=1		
GPIO_18	12	GPIO_AP_FROM_DISPLAY_PANEL_ID	GPIO AP FROM DISPLAY PANEL ID	MAKE_BASE=TRUE	IN	47
GPIO_19	12	PP1V8_IO	PP1V8 IO	PMU_ID: AVUS=1, WHITNEY = NC		
GPIO_20	12	NC_AP_GPIO20	NC AP GPIO20	MAKE_BASE=TRUE NO_TEST=1		
GPIO_21	12	NC_AP_GPIO21	NC AP GPIO21	MAKE_BASE=TRUE NO_TEST=1		
GPIO_22	12	GPIO_AP_TO_NFC_DEV_WAKE	GPIO AP TO NFC DEV WAKE	MAKE_BASE=TRUE	OUT	38
GPIO_23	12	NC_AP_GPIO23	NC AP GPIO23	MAKE_BASE=TRUE NO_TEST=1		
GPIO_24	12	GPIO_AP_FROM_CODEC_INT_L	GPIO AP FROM CODEC INT L	MAKE_BASE=TRUE	IN	5 31
GPIO_25	12	GPIO_AP_FROM_SPKRAMP_TOP_INT_L	GPIO AP FROM SPKRAMP TOP INT L	MAKE_BASE=TRUE	IN	38
GPIO_26	12	GPIO_AP_TO_SPKRAMP_TOP_RESET_L	GPIO AP TO SPKRAMP TOP RESET L	MAKE_BASE=TRUE	OUT	38
GPIO_27	12	GPIO_AP_FROM_BT_AUDIO_SYNC	GPIO AP FROM BT AUDIO SYNC	MAKE_BASE=TRUE	IN	38
GPIO_28	12	GPIO_AP_TO_AMUX_PMU_SYNC	GPIO AP TO AMUX PMU SYNC	MAKE_BASE=TRUE	OUT	22
GPIO_29	12	GPIO_AP_TO_TOUCH_RESET_L	GPIO AP TO TOUCH RESET L	MAKE_BASE=TRUE	OUT	48
GPIO_30	12	NC_AP_GPIO30	NC AP GPIO30	MAKE_BASE=TRUE NO_TEST=1		
GPIO_31	12	NC_AP_GPIO31	NC AP GPIO31	MAKE_BASE=TRUE NO_TEST=1		

SOC: Misc

7	NC_AP_TMR32_PWM0	NC_AP_TMR32_PWM0	MAKE_BASE=TRUE NO_TEST=1
7	NC_AP_TMR32_PWM1	NC_AP_TMR32_PWM1	MAKE_BASE=TRUE NO_TEST=1
7	NC_AP_TMR32_PWM2	NC_AP_TMR32_PWM2	MAKE_BASE=TRUE NO_TEST=1
7	NC_PAD_MTR_VREF_POS	NC_PAD_MTR_VREF_POS	MAKE_BASE=TRUE NO_TEST=1
7	NC_PAD_MTR_VREF_NEG	NC_PAD_MTR_VREF_NEG	MAKE_BASE=TRUE NO_TEST=1
7	NC_USB_ID_AP	NC_USB_ID_AP	MAKE_BASE=TRUE NO_TEST=1

SOC: PCIe

8	NC_PCIE1_AP_CLKREQ_L	NC_PCIE1_AP_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE1_AP_REF_CLK_P	NC_PCIE1_AP_REF_CLK_P	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE1_AP_REF_CLK_N	NC_PCIE1_AP_REF_CLK_N	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE1_AP_RX_P	NC_PCIE1_AP_RX_P	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE1_AP_RX_N	NC_PCIE1_AP_RX_N	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE1_AP_TX_P	NC_PCIE1_AP_TX_P	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE1_AP_TX_N	NC_PCIE1_AP_TX_N	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE1_AP_RESET_L	NC_PCIE1_AP_RESET_L	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE2_CLKREQ_L	NC_PCIE2_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE2_AP_REF_CLK_P	NC_PCIE2_AP_REF_CLK_P	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE2_AP_REF_CLK_N	NC_PCIE2_AP_REF_CLK_N	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE2_AP_RX_P	NC_PCIE2_AP_RX_P	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE2_AP_RX_N	NC_PCIE2_AP_RX_N	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE2_AP_TX_P	NC_PCIE2_AP_TX_P	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE2_AP_TX_N	NC_PCIE2_AP_TX_N	MAKE_BASE=TRUE NO_TEST=1
8	NC_PCIE2_AP_RESET_L	NC_PCIE2_AP_RESET_L	MAKE_BASE=TRUE NO_TEST=1

SOC: ISP

9	NC_LPDP_ISP_AUX_RX_D1P	NC_LPDP_ISP_AUX_RX_D1P	MAKE_BASE=TRUE NO_TEST=1
9	NC_LPDP_ISP_AUX_RX_D3P	NC_LPDP_ISP_AUX_RX_D3P	MAKE_BASE=TRUE NO_TEST=1
9	NC_LPDP_ISP_AUX_RX_D4P	NC_LPDP_ISP_AUX_RX_D4P	MAKE_BASE=TRUE NO_TEST=1
9	NC_LPDP_ISP_AUX_RX_D6P	NC_LPDP_ISP_AUX_RX_D6P	MAKE_BASE=TRUE NO_TEST=1
9	NC_LPDP_ISP_AUX_RX_D7P	NC_LPDP_ISP_AUX_RX_D7P	MAKE_BASE=TRUE NO_TEST=1
9	NC_LPDP_ISP_AUX_RX_D8P	NC_LPDP_ISP_AUX_RX_D8P	MAKE_BASE=TRUE NO_TEST=1
9	NC_LPDP_ISP_AUX_RX_D10P	NC_LPDP_ISP_AUX_RX_D10P	MAKE_BASE=TRUE NO_TEST=1
9	NC_LPDP_ISP_AUX_RX_D11P	NC_LPDP_ISP_AUX_RX_D11P	MAKE_BASE=TRUE NO_TEST=1
9	NC_I2C1_ISP_SCL	NC_I2C1_ISP_SCL	MAKE_BASE=TRUE NO_TEST=1
9	NC_I2C1_ISP_SDA	NC_I2C1_ISP_SDA	MAKE_BASE=TRUE NO_TEST=1
9	NC_ISP_GPIO6	NC_ISP_GPIO6	MAKE_BASE=TRUE NO_TEST=1
9	NC_ISP_GPIO7	NC_ISP_GPIO7	MAKE_BASE=TRUE NO_TEST=1

SOC: Display

10	NC_LPDP_AP_TX0P	NC_LPDP_AP_TX0P	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_TX0N	NC_LPDP_AP_TX0N	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_TX1P	NC_LPDP_AP_TX1P	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_TX1N	NC_LPDP_AP_TX1N	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_TX2P	NC_LPDP_AP_TX2P	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_TX2N	NC_LPDP_AP_TX2N	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_TX3P	NC_LPDP_AP_TX3P	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_TX3N	NC_LPDP_AP_TX3N	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_AUXP	NC_LPDP_AP_AUXP	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_AUXN	NC_LPDP_AP_AUXN	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_RCALP	NC_LPDP_AP_RCALP	MAKE_BASE=TRUE NO_TEST=1
10	NC_LPDP_AP_RCALN	NC_LPDP_AP_RCALN	MAKE_BASE=TRUE NO_TEST=1
10	NC_I2C_DISP_SCL	NC_I2C_DISP_SCL	MAKE_BASE=TRUE NO_TEST=1
10	NC_I2C_DISP_SDA	NC_I2C_DISP_SDA	MAKE_BASE=TRUE NO_TEST=1
10	NC_TOUCH_BSYNC0_DISP	NC_TOUCH_BSYNC0_DISP	MAKE_BASE=TRUE NO_TEST=1
10	NC_TOUCH_BSYNC1_DISP	NC_TOUCH_BSYNC1_DISP	MAKE_BASE=TRUE NO_TEST=1
10	NC_POL_DISP	NC_POL_DISP	MAKE_BASE=TRUE NO_TEST=1
10	NC_WAKEUP_DP_DISP	NC_WAKEUP_DP_DISP	MAKE_BASE=TRUE NO_TEST=1
10	NC_EDP_HPD_DISP	NC_EDP_HPD_DISP	MAKE_BASE=TRUE NO_TEST=1

SOC: Serial

11	NC_UART1_AP_CTS_1V2_L	NC_UART1_AP_CTS_1V2_L	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART1_AP_RTS_1V2_L	NC_UART1_AP_RTS_1V2_L	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART1_AP_RXD_1V2	NC_UART1_AP_RXD_1V2	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART1_AP_TXD_1V2	NC_UART1_AP_TXD_1V2	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART2_AP_CTS_L	NC_UART2_AP_CTS_L	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART2_AP_RTS_L	NC_UART2_AP_RTS_L	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART2_AP_RXD	NC_UART2_AP_RXD	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART2_AP_TXD	NC_UART2_AP_TXD	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART3_AP_CTS_L	NC_UART3_AP_CTS_L	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART3_AP_RTS_L	NC_UART3_AP_RTS_L	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART3_AP_RXD	NC_UART3_AP_RXD	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART3_AP_TXD	NC_UART3_AP_TXD	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART6_AP_RXD	NC_UART6_AP_RXD	MAKE_BASE=TRUE NO_TEST=1
11	NC_UART6_AP_TXD	NC_UART6_AP_TXD	MAKE_BASE=TRUE NO_TEST=1
11	NC_I2S1_AP_MCLK	NC_I2S1_AP_MCLK	MAKE_BASE=TRUE NO_TEST=1
11	NC_I2S2_AP_MCLK	NC_I2S2_AP_MCLK	MAKE_BASE=TRUE NO_TEST=1
11	NC_I2S3_AP_DIN	NC_I2S3_AP_DIN	MAKE_BASE=TRUE NO_TEST=1
11	NC_I2S3_AP_DOUT	NC_I2S3_AP_DOUT	MAKE_BASE=TRUE NO_TEST=1
11	NC_I2S3_AP_BCLK	NC_I2S3_AP_BCLK	MAKE_BASE=TRUE NO_TEST=1
11	NC_I2S3_AP_LRCLK	NC_I2S3_AP_LRCLK	MAKE_BASE=TRUE NO_TEST=1
11	NC_I2S3_AP_MCK	NC_I2S3_AP_MCK	MAKE_BASE=TRUE NO_TEST=1
11	NC_PDM_AP_OUT_DAT	NC_PDM_AP_OUT_DAT	MAKE_BASE=TRUE NO_TEST=1
11	NC_SPI4_MISO_AP	NC_SPI4_MISO_AP	MAKE_BASE=TRUE NO_TEST=1
11	NC_SPI4_SCLK_AP	NC_SPI4_SCLK_AP	MAKE_BASE=TRUE NO_TEST=1

SOC: AON

13	NC_CLK_CLK24M_OUT	NC_CLK_CLK24M_OUT	MAKE_BASE=TRUE NO_TEST=1
13	NC_SPI1_AOP_MISO	NC_SPI1_AOP_MISO	MAKE_BASE=TRUE NO_TEST=1
13	NC_SPI1_AOP_MOSI	NC_SPI1_AOP_MOSI	MAKE_BASE=TRUE NO_TEST=1
13	NC_SPI1_AOP_SCLK	NC_SPI1_AOP_SCLK	MAKE_BASE=TRUE NO_TEST=1

Rcpt: 516S00529 <-- This one on MLB
Plug: 516S00528

JUAT
MM3531-2700A22
F-ST-SM

Pin	Net	Pin	Net
1		12	50_ANT6 (GND_VOID=TRUE)
2		13	
3		14	50_R1_AOA1 (GND_VOID=TRUE)
4	UAT_SAWTOOTH_A_B2B	15	
5		16	50_R1_AOA3 (GND_VOID=TRUE)
6		17	
7		18	50_ANT2 (GND_VOID=TRUE)
8		19	
9		20	50_R1_AOA0 (GND_VOID=TRUE)
10		21	
11	UAT_SAWTOOTH_B_B2B	22	50_ANT4 (GND_VOID=TRUE)
SHLD			
23		29	
24		30	
25		31	
26		32	
27		33	
28		34	

ROOM=RF_UAT

علي البحر فريق الهارد حلب تك

I218

Net	Pin	Pin	Net
50_WLAN_A_TX0	50_WLAN_A_TX0	PP_VDD_MAIN	PP_VDD_MAIN
50_WLAN_A_RX0_LAA	50_WLAN_A_RX0	PP1V8_S2	PP1V8_S2 (PP1V8_S2 :FEM Imax = 40mA)
50_WLAN_A_TX1	50_WLAN_A_TX1	PP1V8_S4	PP1V8_S4 (PP1V8_S4 :FEM Imax = 40mA)
50_WLAN_A_RX1_LAA	50_WLAN_A_RX1	50_LAA_TO_ANT_LAT	50_LAA_TO_ANT_LAT
		50_LAA_TO_ANT_UAT	50_LAA_TO_ANT_UAT
5GHZ_C0_VDET	5GHZ_C0_VDET		
5GHZ_C1_VDET	5GHZ_C1_VDET	50_LAA_TO_XCVR_LAT	50_LAA_TO_XCVR_LAT
		50_LAA_TO_XCVR_UAT	50_LAA_TO_XCVR_UAT
RFA0_SW_CTRL0	RFA0_SW_CTRL0		
RFA0_SW_CTRL1	RFA0_SW_CTRL1	RFFE_LAA_LAT_VIO	VIO_RFFE_XCVR_TO_RX_1V8
RFA0_SW_CTRL2	RFA0_SW_CTRL2	RFFE_LAA_LAT_CLK	RFFE_XCVR_TO_FE_RX_CLK
RFA1_SW_CTRL0	RFA1_SW_CTRL0	RFFE_LAA_LAT_DATA	RFFE_XCVR_TO_FE_RX_DATA
RFA1_SW_CTRL1	RFA1_SW_CTRL1	RFFE_LAA_UAT_VIO	RFFE_LAA_UAT_VIO
RFA1_SW_CTRL2	RFA1_SW_CTRL2	RFFE_LAA_UAT_CLK	RFFE_LAA_UAT_CLK
		RFFE_LAA_UAT_DATA	RFFE_LAA_UAT_DATA
		50_LAA_TO_R1	50_LAA_TO_R1
		R1_TO_BB_LAA_SW_CTRL	IO_R1_TO_BB_LAA_SW_CTRL

LAA_MLB

C9003 4UF 20% 6.3V CERM-X5R 0201 ROOM=LAT_FEM PLACE_NEAR=U_5G_L_W:19:3MM
C9004 4UF 20% 6.3V CERM-X5R 0201 ROOM=LAT_FEM PLACE_NEAR=U_5G_L_W:19:3MM
C9005 4UF 20% 6.3V CERM-X5R 0201 ROOM=LAT_FEM PLACE_NEAR=U_5G_L_W:19:3MM

I219

Net	Pin	Pin	Net
50_LAA_TO_ANT_UAT	50_LAA_TO_ANT_UAT	VFE_LO_1V2	VFE_LO_1V2
50_LAA_TO_ANT_LAT	50_LAA_TO_ANT_LAT	VFE_HI_3V15	VFE_HI_3V15
50_WLAN_G_LAT	50_WLAN_G_LAT	VPA_ET_HB	VPA_ET_HB
		VPA_ET_UHB	VPA_ET_UHB
50_R1_ANT_CH9	50_R1_ANT_CH9	VPA_2G	VPA_2G
		VIO_RFFE_XCVR_TO_TX_1V8	VIO_RFFE_XCVR_TO_TX_1V8
		VIO_RFFE_XCVR_TO_RX_1V8	VIO_RFFE_XCVR_TO_RX_1V8
		RFFE_XCVR_TO_LBTX_CLK	RFFE_XCVR_TO_LBTX_CLK
		RFFE_XCVR_TO_LBTX_DATA	RFFE_XCVR_TO_LBTX_DATA
		RFFE_XCVR_TO_HBTX_CLK	RFFE_XCVR_TO_HBTX_CLK
		RFFE_XCVR_TO_HBTX_DATA	RFFE_XCVR_TO_HBTX_DATA
		RFFE_XCVR_TO_FE_RX_CLK	RFFE_XCVR_TO_FE_RX_CLK
		RFFE_XCVR_TO_FE_RX_DATA	RFFE_XCVR_TO_FE_RX_DATA
		50_XCVR_TX0_HB	50_XCVR_TX0_HB
		50_XCVR_TX0_MB3	50_XCVR_TX0_MB3
		50_XCVR_TX1_HB	50_XCVR_TX1_HB
		50_XCVR_TX1_MB1	50_XCVR_TX1_MB1
		50_XCVR_TX0_MB2	50_XCVR_TX0_MB2
		50_XCVR_TX0_LB2	50_XCVR_TX0_LB2
		50_XCVR_TX0_MB1	50_XCVR_TX0_MB1
		50_XCVR_TX1_UHB	50_XCVR_TX1_UHB
		50_XCVR_RX2_UHB_PRX	50_XCVR_RX2_UHB_PRX
		50_XCVR_RX6_MB_UHB_PRX	50_XCVR_RX6_MB_UHB_PRX
		50_XCVR_RX8_MLB_HB_PRX	50_XCVR_RX8_MLB_HB_PRX
		50_XCVR_RX9_MLB_HB_PRX	50_XCVR_RX9_MLB_HB_PRX
		50_XCVR_RX10_MLB_HB_PRX	50_XCVR_RX10_MLB_HB_PRX
		50_XCVR_RX14_LB_MLB_PRX	50_XCVR_RX14_LB_MLB_PRX
		50_MMDSM_MHB_ANT	50_MMDSM_MHB_ANT
		50_MMDSM_UHB_ANT	50_MMDSM_UHB_ANT
		50_ANT2	50_ANT2
		50_ANT4	50_ANT4
		50_ANT6_UHB	50_ANT6_UHB
		50_HBPA_ANT3	50_HBPA_ANT3
		50_HBPA_DRX_OUT	50_HBPA_DRX_OUT
		50_LB_TX_ANT1	50_LB_TX_ANT1
		50_UHBPA_2G_LB_OUT	50_UHBPA_2G_LB_OUT
		50_UHBPA_UHB	50_UHBPA_UHB
		50_CPLL_CPLOUT1	50_CPLL_CPLOUT1
		50_CPLL_CPLOUT2	50_CPLL_CPLOUT2
50_ANT2	50_ANT2	LAT_SUBUS_A	LAT_SAWTOOTH_A
50_ANT4	50_ANT4	LAT_SUBUS_B	LAT_SAWTOOTH_B
50_ANT6	50_ANT6	UAT_SUBUS_A	UAT_SAWTOOTH_A
PP3V0_S2	PP3V0_S2	UAT_SUBUS_B	UAT_SAWTOOTH_B
UAT_SAWTOOTH_A_B2B	UAT_SUBUS_A_B2B		
UAT_SAWTOOTH_B_B2B	UAT_SUBUS_B_B2B		

RADIO_MLB_ICE_LOFT

I223

Net	Pin	Pin	Net
PP1V8_S4	PP1V8_S4		
PP1V0_R1_ANA_S4	PP1V0_R1_ANA		
PP1V0_S4	PP1V0_R1_SOC		
GPIO_PMU_TO_R1_RESET_L (IN)	APPMU_TO_R1_RESET_L		
CLK_GPIO_PMU_TO_WLAN_R1_32K (IN)	APPMU_TO_WLAN_32K_CLK		
GPIO_AOP_TO_R1_COREDUMP_TRIGGER (IN)	AOP_TO_R1_COREDUMP_TRIG		
Freq SPI: 10MHz			
GPIO_AOP_TO_R1_SPI_CS_L (IN)	SPI_AOP_TO_R1_CS_L		
SPI0_AOP_TO_IMU_R1_SCLK (IN)	SPI_AOP_TO_R1_SCLK		
SPI0_AOP_TO_IMU_R1_MOSI (IN)	SPI_AOP_TO_R1_MOSI		
SPI0_AOP_FROM_IMU_R1_MISO (OUT)	SPI_R1_TO_AOP_MISO		
GPIO_AOP_FROM_R1_INT	R1_TO_AOP_INT		
I2C_R1_TO_NFC_SCL	I2C_R1_TO_SE_SCL		
I2C_R1_BI_NFC_SDA	I2C_R1_TO_SE_SDA (ROOM=MLB)		
IO_BB_TO_R1_COEX	BB_TO_R1_COEX (ROOM=R1)		
IO_WLAN_TO_R1_COEX	WLAN_TO_R1_COEX		
IO_R1_TO_WLAN_COEX	R1_TO_WLAN_COEX		
GPIO_AOP_TO_R1_TIME_SYNC (IN)	AOP_TO_R1_TIME_SYNC		
IO_BT_TO_R1_TIME_SYNC	BT_TO_R1_TIME_SYNC		
GPIO_BT_TO_R1_DEV_WAKE	BT_TO_R1_WAKE		
SWD_NUB_BI_R1_SWDIO (BI)	SWD_AOP_BI_R1_SWDIO		
SWD_NUB_TO_MANY_SWCLK (IN)	SWD_AOP_TO_MANY_SWCLK		
50_R1_AOA1	50_R1_ANT0		
50_R1_AOA3	50_R1_ANT1		
50_R1_AOA0	50_R1_ANT3		
50_R1_ANT_CH9	50_R1_ANT_CH9		
50_LAA_TO_R1	50_LAA_TO_R1		
NC_R1_TUNER_GPO1 (NO_TEST=1)	R1_TUNER_GPO1		
NC_R1_TUNER_GPO2 (NO_TEST=1)	R1_TUNER_GPO2		
IO_R1_TO_BB_LAA_SW_CTRL	R1_TO_BB_LAA_SW_CTRL		

POWER UP SEQUENCE: Assert PMU_TO_R1_RESET_L >500uS after PP1V8_S4 AND PP1V0_S4 rails

RADIO PA NTC

C3043 100PF 5% 16V NP0-C0G 01005-1 ROOM=PMU

I229 R3043 10KOHM-1% 01005 ROOM=PMU

NTC_RADIO_PA_P
NTC_RADIO_PA_N

OMIT XW3043 SHORT-20L-0.05MM-SM ROOM=PMU

SCHAND (E.P.S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	LAT_SAWTOOTH*, UAT_SAWTOOTH*

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RFFE_SHIELD	S	A_DIELECTRIC_2X	LAT_SAWTOOTH*, UAT_SAWTOOTH*	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_100UM	P	PWR_100UM	PP1V8_S4	?
PWR_SHAPE	P	PWR_SHAPE	PP1V0_S4	?
PWR_200UM	P	PWR_200UM	PP1V0_R1_ANA_S4	?

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
S_PWR_100UM	S	100UM-249UM_SPACING	PP1V8_S4	?
S_PWR_SHAPE	S	250UM+_SPACING	PP1V0_S4	?
S_PWR_200UM	S	100UM-249UM_SPACING	PP1V0_R1_ANA_S4	?

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN MEGAHERTZ.

ICE19.1 RADIO_MLB_LOFT

LAST_MODIFICATION=Fri May 3 22:17:25 2019

PAGE	CSA	CONTENTS	SYNC	DATE
59	1	SCH,RADIO_MLB_ICE_LOFT		
60	2	HB SPAD		05/01/2018
61	3	UHB MLB SPAD		05/01/2018
62	4	LOWER COUPLER		05/01/2018
63	5	LOWER ANTENNA FEEDS		05/01/2018
64	6	ANTENNA SYSTEM		05/01/2018

64 58 IO 50_LAA_TO_ANT_UAT
63 58 IO 50_LAA_TO_ANT_LAT

63 58 IO 50_WLAN_G_LAT

58 64 IO 50_R1_ANT_CH9

61 60 58 VFE_LO_1V2
62 61 60 58 VFE_HI_3V15

60 58 VPA_ET_HB
61 58 VPA_ET_UHB
61 58 VPA_2G

62 61 60 58 VIO_RFFE_XCVR_TO_TX_1V8
61 60 58 VIO_RFFE_XCVR_TO_RX_1V8
62 61 58 RFFE_XCVR_TO_LBTX_CLK
62 61 58 RFFE_XCVR_TO_LBTX_DATA
61 60 58 RFFE_XCVR_TO_HBTX_CLK
61 60 58 RFFE_XCVR_TO_HBTX_DATA
61 60 58 RFFE_XCVR_TO_FE_RX_CLK
61 60 58 RFFE_XCVR_TO_FE_RX_DATA

60 58 50_XCVR_TX0_HB
60 58 50_XCVR_TX0_MB3
60 58 50_XCVR_TX1_HB
60 58 50_XCVR_TX1_MB1
61 58 50_XCVR_TX0_MB2
61 58 50_XCVR_TX0_LB2
61 58 50_XCVR_TX0_MB1
61 58 50_XCVR_TX1_UHB

61 58 50_XCVR_RX2_UHB_PRX
60 58 50_XCVR_RX6_MB_UHB_PRX
60 58 50_XCVR_RX8_MLB_HB_PRX
60 58 50_XCVR_RX9_MLB_HB_PRX
60 58 50_XCVR_RX10_MLB_HB_PRX
61 58 50_XCVR_RX14_LB_MLB_PRX

60 58 50_MMDSM_MHB_ANT
61 58 50_MMDSM_UHB_ANT

59 58 50_ANT2
59 58 50_ANT4
64 58 50_ANT6
60 58 50_HBPA_ANT3
60 58 50_HBPA_DRX_OUT
63 58 50_LB_TX_ANT1
61 58 50_UHBPA_2G_LB_OUT
61 58 50_UHBPA_UHB

59 58 50_ANT2
59 58 50_ANT4
59 58 50_ANT6

59 58 PP3V0_S2

59 58 UAT_SAWTOOTH_A_B2B
59 58 UAT_SAWTOOTH_B_B2B

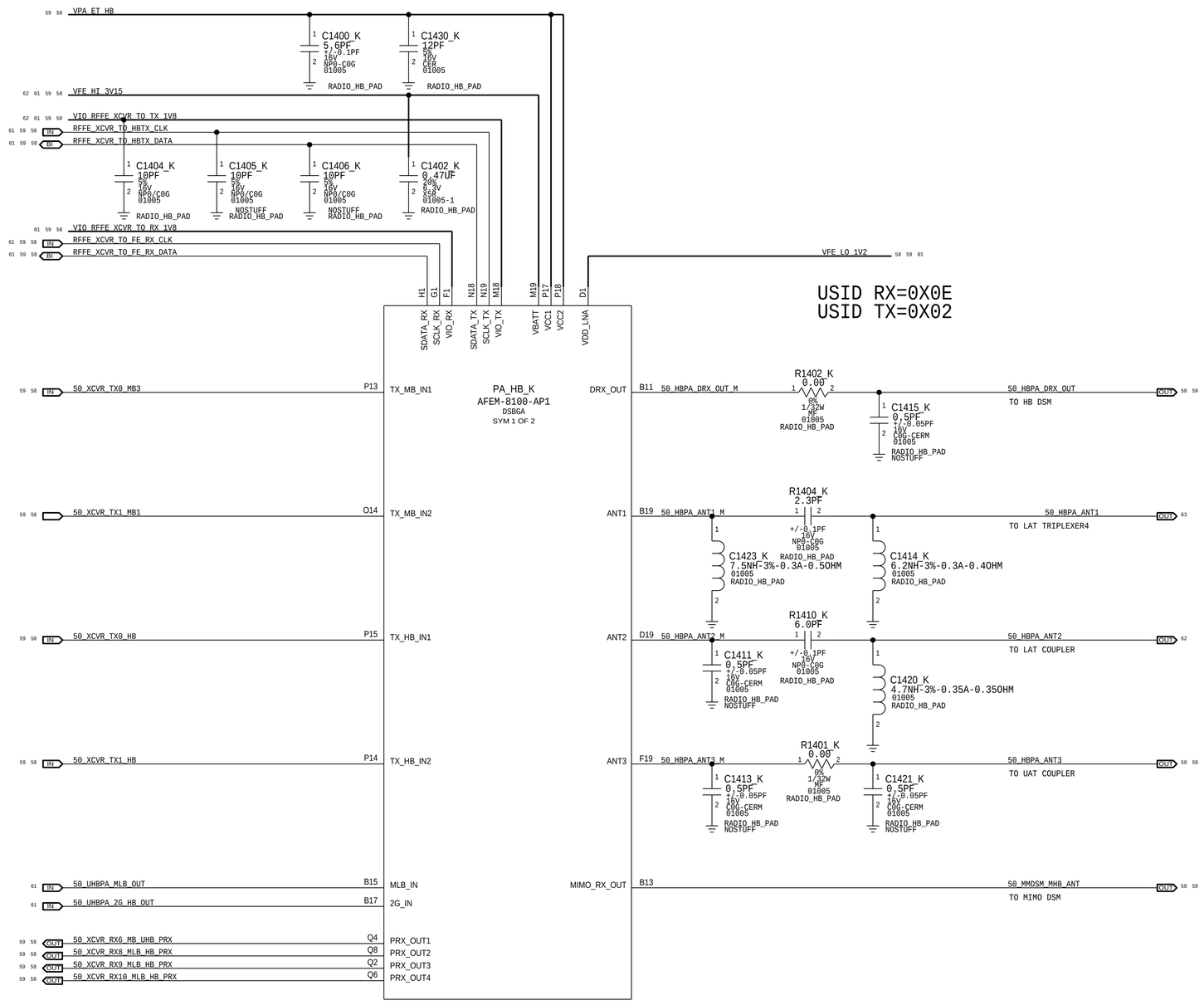
62 58 50_CPLL_CPLOUT1
62 58 50_CPLL_CPLOUT2

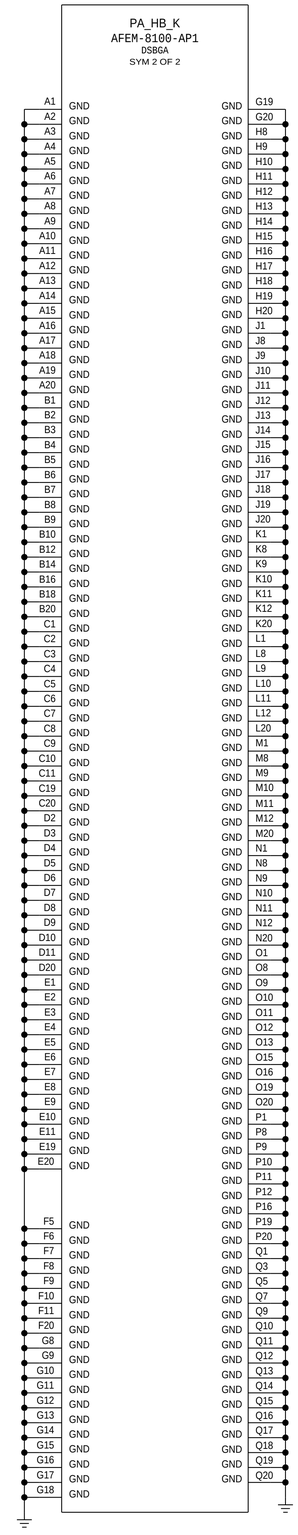
64 58 LAT_SAWTOOTH_A
64 58 LAT_SAWTOOTH_B
64 58 UAT_SAWTOOTH_A
64 58 UAT_SAWTOOTH_B

CLASS TO CLASS SPACING

CLASS NAME	CLASS NAME	CONSTRAINT SET
50_WIDE	50_WIDE	A_DIELECTRIC_4XV_50_WIDE_SE
50_WIDE	50_THIN	A_DIELECTRIC_4XD_50_WIDE_SE
50_WIDE	50_THIN_UNSHIELDED	A_DIELECTRIC_4XD_50_WIDE_SE
50_THIN	50_THIN	A_DIELECTRIC_4XD_50_THIN_SE
50_THIN	50_THIN_UNSHIELDED	A_DIELECTRIC_4XD_50_THIN_SE
50_THIN_UNSHIELDED	50_THIN_UNSHIELDED	A_DIELECTRIC_2X
50_WIDE_L1_THIN	50_WIDE	A_DIELECTRIC_4XV_50_WIDE_SE
50_WIDE_L1_THIN	50_THIN	A_DIELECTRIC_4XD_50_WIDE_L1_THIN_SE
50_WIDE_L1_THIN	50_THIN_UNSHIELDED	A_DIELECTRIC_4XD_50_WIDE_L1_THIN_SE
RF_SHIELD	GND	DEFAULT
RF_SHIELD	RF_SHIELD	A_DIELECTRIC_2XD
RFFE_SHIELD	GND	DEFAULT
RFFE_SHIELD	RFFE_SHIELD	DEFAULT

HB SPAD





CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	S/A	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RFFE_SHIELD	S	A_DIELECTRIC_2X	*RFFE*, VIO_RFFE*	Y

DOMAIN (P,F,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_XCVR*, 50_HBPA_DRX_OUT_M
P	A_50_WIDE_L1_THIN_SE	50_HBPA_ANT2*, 50_HBPA_ANT3*, 50_HBPA_ANT1*, 50_HBPA_DRX_OUT

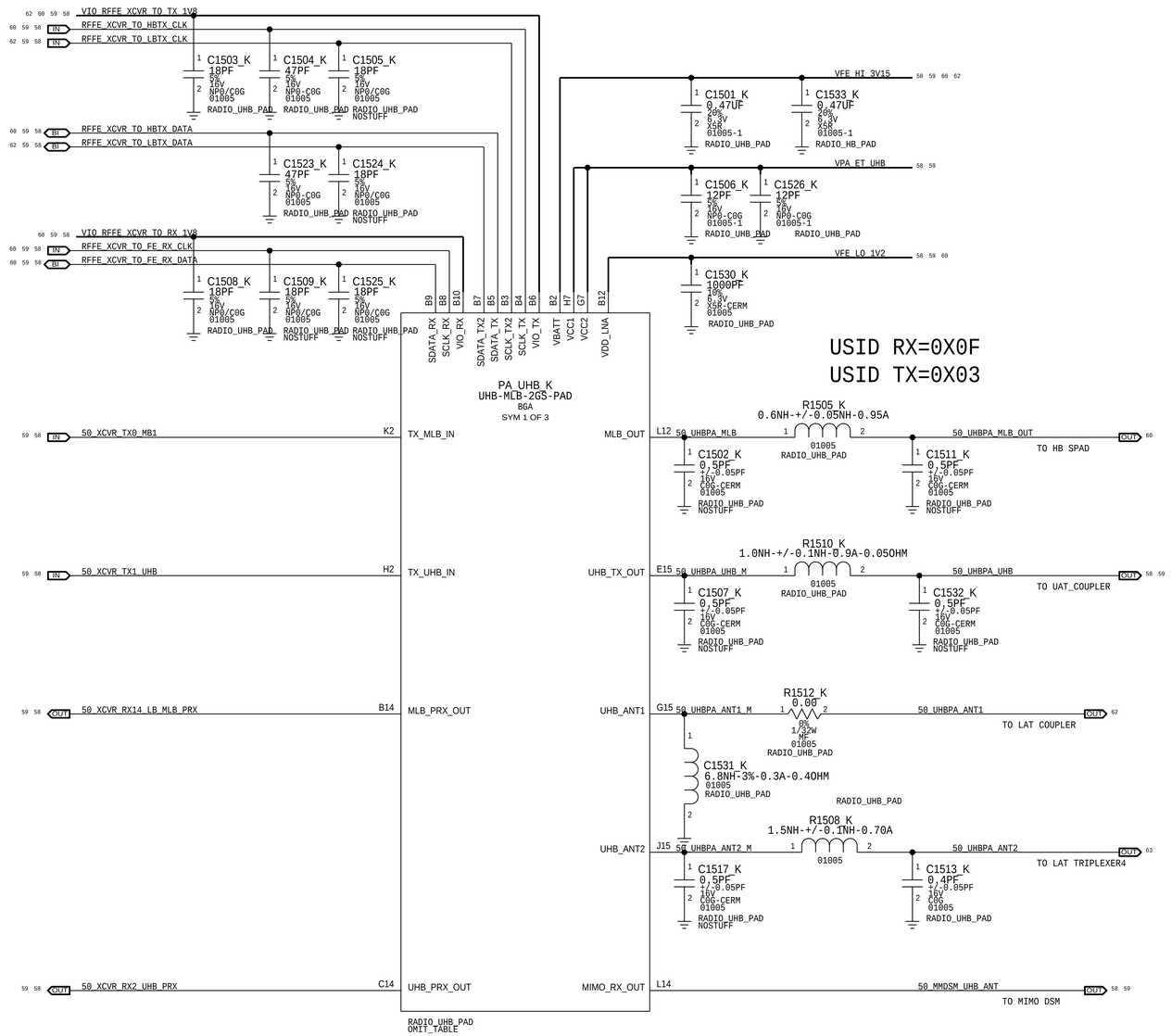
DOMAIN (P,F,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_200UM	VFE_HI_3V15
P	PWR_100UM	VFE_LO_1V2, VIO_RFFE*
P	PWR_SHAPE	VPA_ET_HB, VPA_ET_UHB, VPA_2G

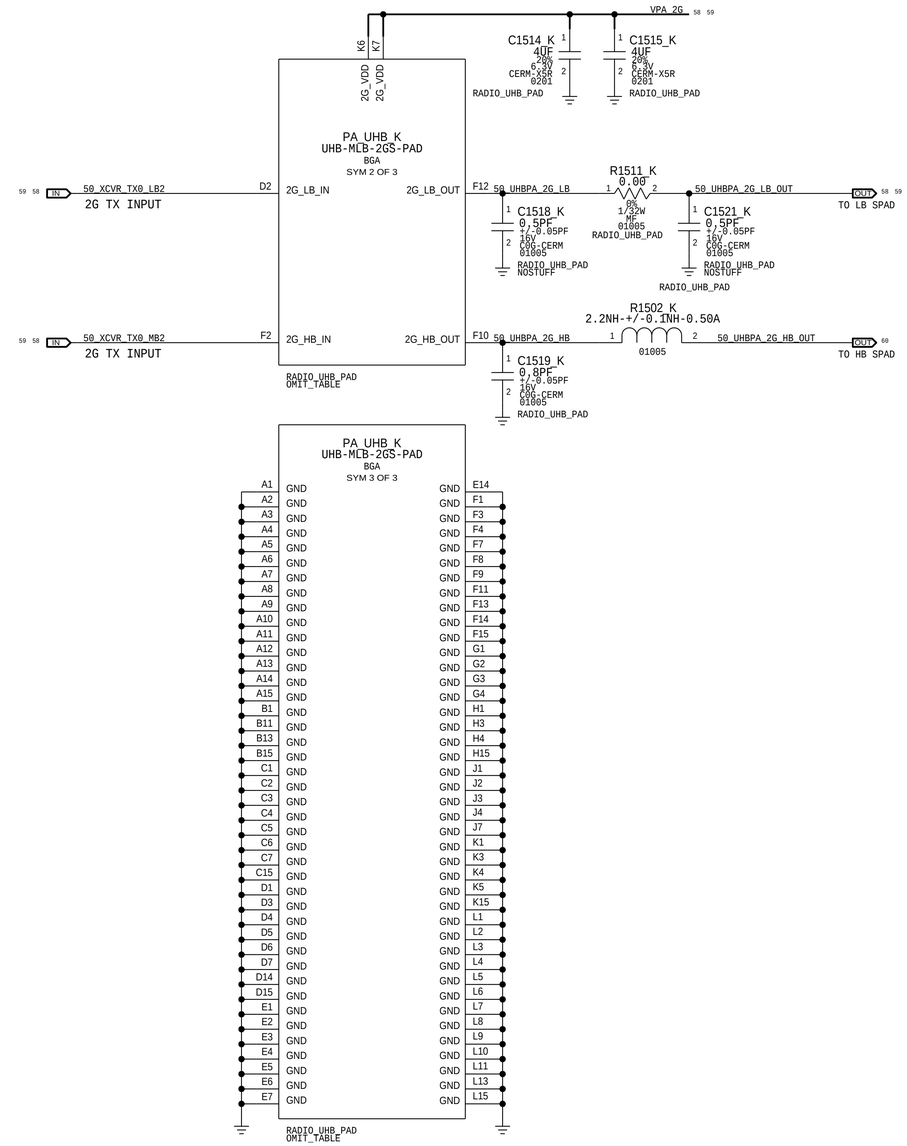
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	S/A	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_XCVR*,50_HBPA_DRX_OUT_M	Y
50_WIDE_L1_THIN	S	A_DIELECTRIC_2X_50_WIDE_L1_THIN_SE	50_HBPA_ANT2*, 50_HBPA_ANT3*	Y
50_WIDE_L1_THIN	S	A_DIELECTRIC_2X_50_WIDE_L1_THIN_SE	50_HBPA_ANT1*, 50_HBPA_DRX_OUT	Y

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSE ONLY - NOT A CHANGE REQUEST

UHB MLB SPAD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S01913	1	SKY78201-18	PA_UHB_K	ROW
353S01914	1	SKY78221-11	PA_UHB_K	USCH



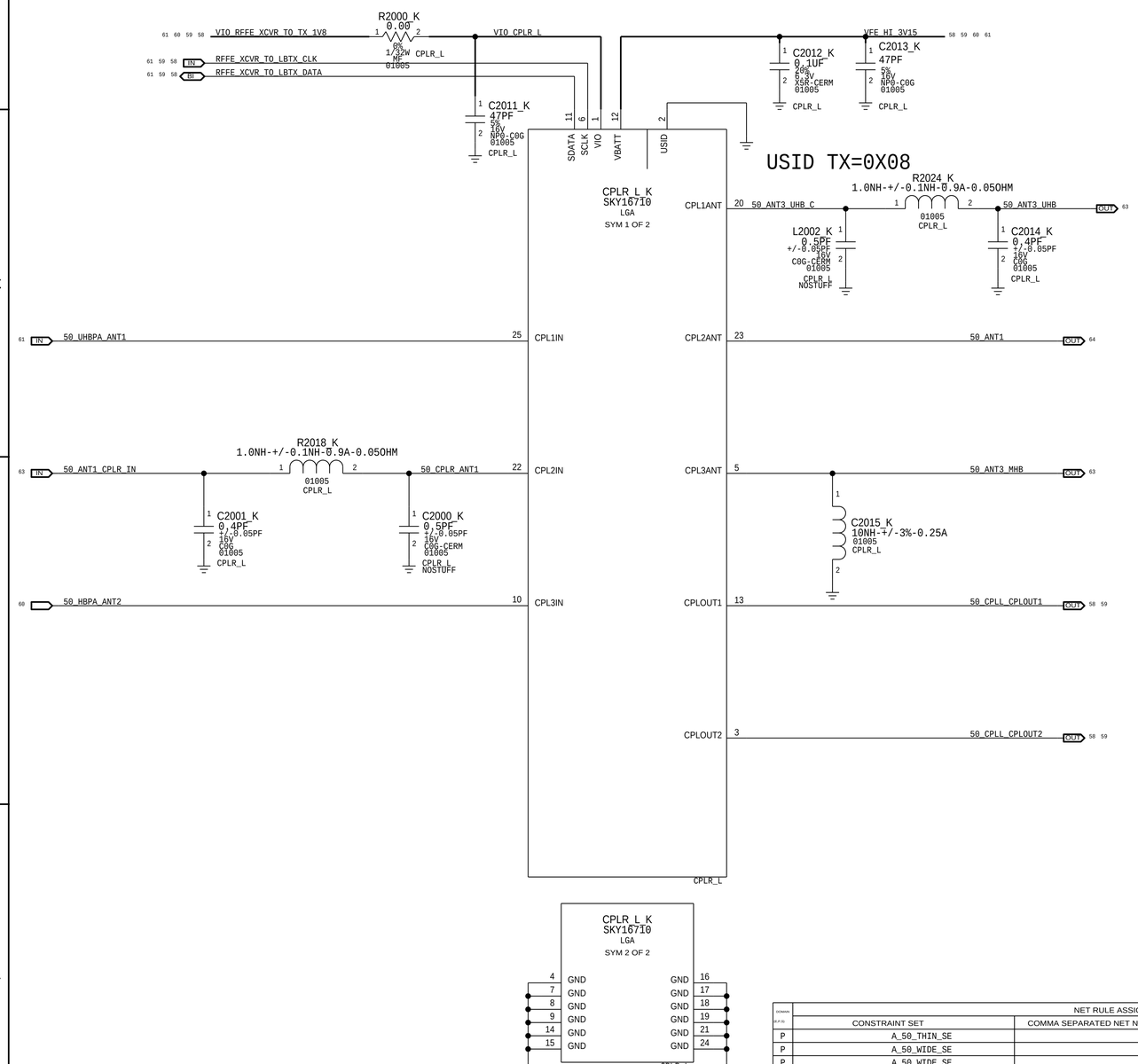


COMMAND (P,F,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_UHBPA_UHB_M, 50_UHBPA_ANT2
P	A_50_THIN_SE	50_UHBPA_MLB, 50_UHBPA_2G_LB*
P	A_50_WIDE_L1_THIN_SE	50_UHBPA_ANT1*, 50_UHBPA_ANT2_M, 50_UHBPA_2G_HB*, 50_UHBPA_UHB, 50_MMDSM*
P	A_50_WIDE_L1_THIN_SE	50_UHBPA_MLB_OUT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CONVERGE
CLASS NAME	TYPE (S,D,T,X)	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_UHBPA_UHB_M, 50_UHBPA_ANT2	Y
50_THIN	S	A_DIELECTRIC_2X	50_UHBPA_MLB, 50_UHBPA_2G_LB*	Y
50_WIDE_L1_THIN	S	A_DIELECTRIC_2X_50_WIDE_L1_THIN_SE	50_UHBPA_ANT1*, 50_UHBPA_ANT2_M, 50_UHBPA_2G_HB*, 50_UHBPA_UHB, 50_MMDSM*	Y
50_WIDE_L1_THIN	S	A_DIELECTRIC_2X_50_WIDE_L1_THIN_SE	50_UHBPA_MLB_OUT	Y

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSE ONLY - NOT A CHANGE REQUEST

LOWER/UPPER COUPLER



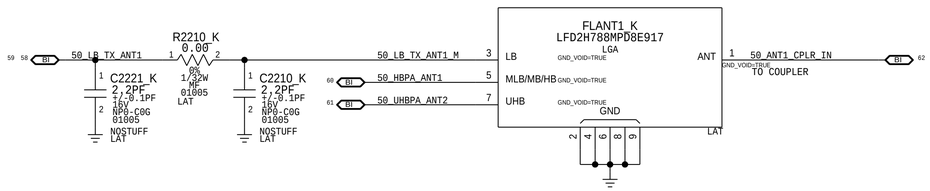
DOMAIN (P,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	VIO_CPLR*

DOMAIN (P,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_CPLL_CPLOUT*
P	A_50_WIDE_SE	50_CPLR_ANT1
P	A_50_WIDE_SE	50_ANT1

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	*** ***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_CPLL_CPLOUT*	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_CPLR_ANT1	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_ANT1	Y

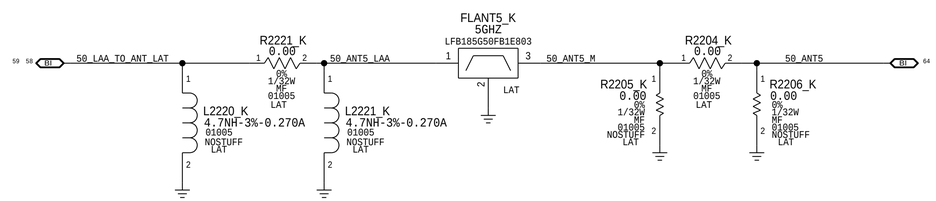
LOWER ANTENNA FEEDS

LB-MHB-UHB TRIPLEXER4



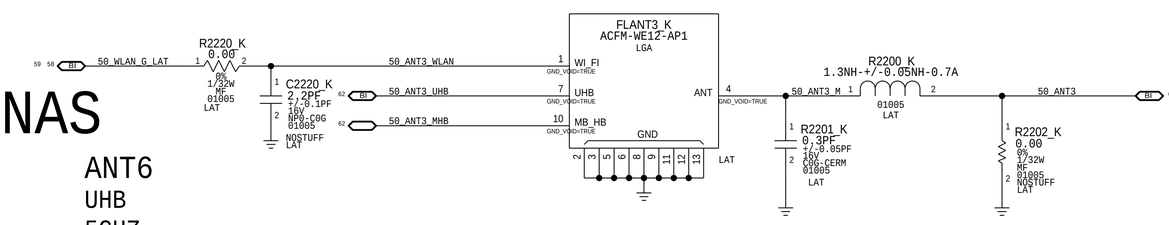
ANT1

5GHZ WLAN BPF



ANT5

MHB-UHB-2.4G TRIPLEXER2



ANT3

UAT ANTENNAS

ANT2	ANT4	ANT6
LB	MB/HB	UHB
LMB/MB/HB	2.4GHZ	5GHZ
L1 GNSS	UHB	

LAT ANTENNAS

ANT1	ANT3	ANT5
LB	MB/HB	5GHZ
LMB/MB/HB	2.4GHZ	
UHB	UHB	

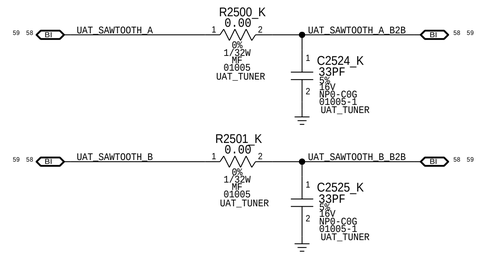
DOMAIN	NET RULE ASSIGNMENT	
P,F,S	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_WIDE_SE	50_ANT5, 50_ANT5_M, 50_LB_TX_ANT1*, 50_ANT3_UHB*
P	A_50_WIDE_SE	50_ANT3, 50_ANT3_M*, 50_ANT3_WLAN
P	A_50_WIDE_SE	50_WLAN_G_LAT
P	A_50_WIDE_SE	50_ANT1_CPLR_IN

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DOMAIN P,F,S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_ANT5, 50_ANT5_M, 50_LB_TX_ANT1*, 50_ANT3_UHB*	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_ANT3, 50_ANT3_M*, 50_ANT3_WLAN	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_WLAN_G_LAT	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_ANT1_CPLR_IN	Y

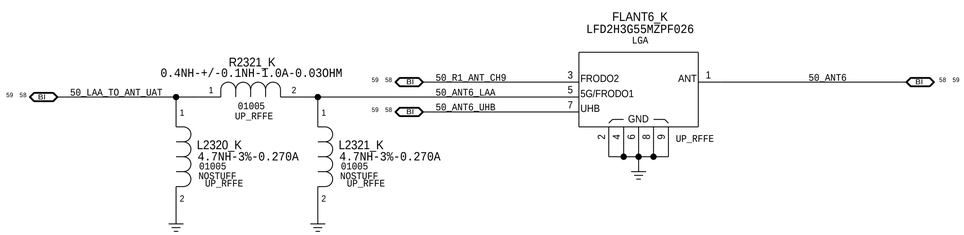
ANTENNA SYSTEM

DOMAIN: P.F.G.	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_WIDE_SE	50_ANT2*, 50_ANT4*, 50_ANT6*, 50_LAA_TO_ANT_UAT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	P.F.G.	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_ANT2*, 50_ANT4*, 50_ANT6*	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_LAA_TO_ANT_UAT	Y

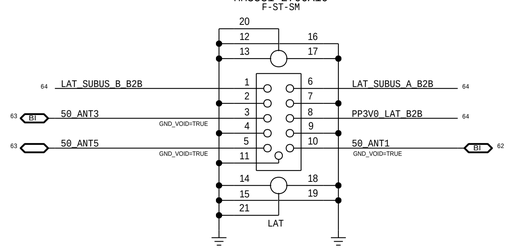


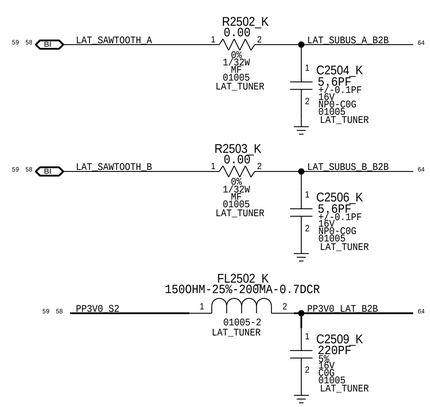
UHB/5G/R



ANT6

LAT





DOMAIN: P.F.G.	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	PP3V0_LAT_B2B

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE ONLY - NOT A CHANGE REQUEST

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

ARROW MLB

LAST_MODIFICATION=Fri May 3 22:17:25 2019

PAGE	CSA	CONTENTS	SYNC	DATE
65 FRONT PAGE	1	FRONT PAGE		
66	2	MODULE		
67	3	FILTERS MATCHING		

POWER
66 58 IO PP1V8_S4
66 58 IO PP1V0_R1_ANA_S4
66 58 IO PP1V0_S4

HOST IPC
66 58 IO SPI0_AOP_TO_IMU_R1_SCLK
66 58 IO GPIO_AOP_TO_R1_SPI_CS_L
66 58 IO SPI0_AOP_FROM_IMU_R1_MISO
66 58 IO SPI0_AOP_TO_IMU_R1_MOSI
66 58 IO GPIO_AOP_TO_R1_COREDUMP_TRIGGER
66 58 IO GPIO_AOP_FROM_R1_INT

RESET/CLOCK
66 58 IO GPIO_PMU_TO_R1_RESET_L
66 58 IO CLK_GPIO_PMU_TO_WLAN_R1_32K
66 58 IO GPIO_AOP_TO_R1_TIME_SYNC

DEBUG
66 58 IO SWD_NUB_TO_MANY_SWCLK
66 58 IO SWD_NUB_BI_R1_SWDIO

SPMI/COEX GPIOS
66 58 IO IO_R1_TO_WLAN_COEX
66 58 IO IO_BB_TO_R1_COEX
66 58 IO IO_WLAN_TO_R1_COEX

SE IPC
66 58 IO I2C_R1_TO_NFC_SCL
66 58 IO I2C_R1_BI_NFC_SDA

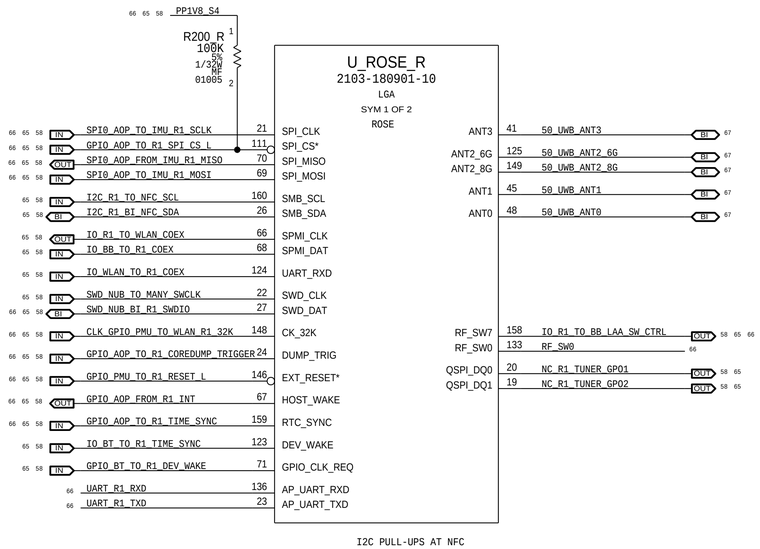
BT TIME SYNC / WAKE
66 58 IO IO_BT_TO_R1_TIME_SYNC
66 58 IO GPIO_BT_TO_R1_DEV_WAKE

ANTENNA SWITCH CTRL
66 58 IO NC_R1_TUNER_GPO1
66 58 IO NC_R1_TUNER_GPO2
66 58 IO IO_R1_TO_BB_LAA_SW_CTRL

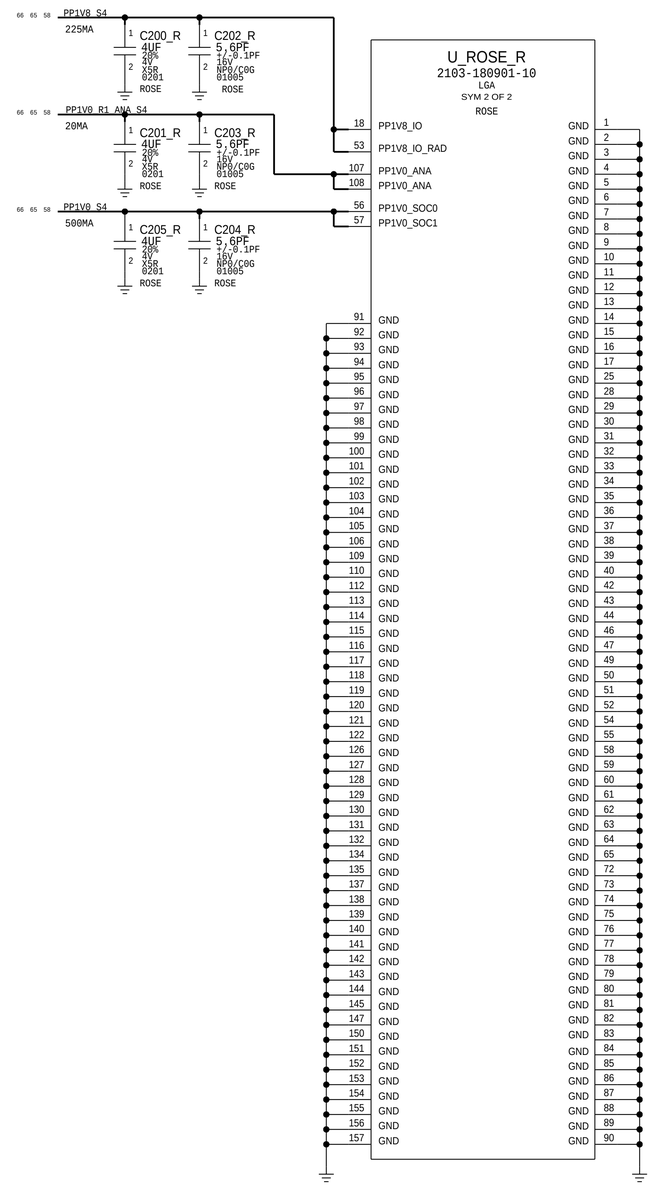
ANTENNA
67 58 IO 50_R1_AOA1
67 58 IO 50_R1_AOA3
67 58 IO 50_R1_AOA0
67 58 IO 50_R1_ANT_CH9
67 58 IO 50_LAA_TO_R1

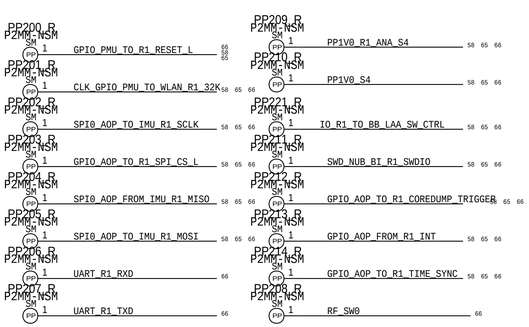
SCH #: 951-07279
PCB #: 920-05369
BOM #: 939-05686

MODULE

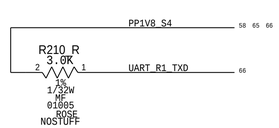


I2C PULL-UPS AT NFC

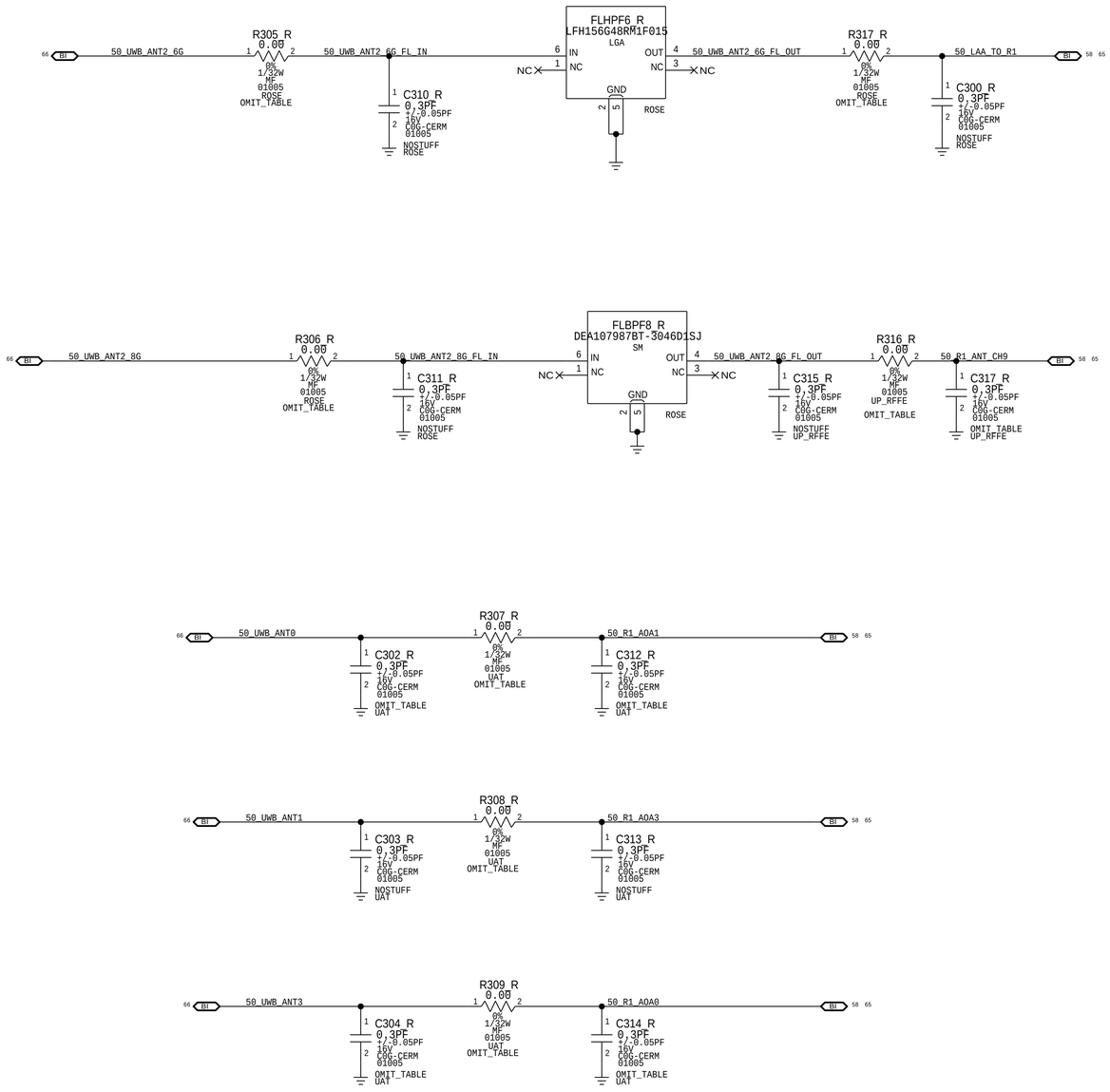




UNSECURE BOOT BOOTSTRAP PULLUP



FILTERS/MATCHING AND ANTENNA



DOMAIN (P,A,D,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_WIDE_SE	50_R1*, 50_UWB*, 50_LAA_TO_R1*

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEARS CHANGED
CLASS NAME	DIFF PAIR	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_R1*, 50_UWB*, 50_LAA_TO_R1* ?	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0161	1	RES,MF,0 OHM,1/32W,01005	R305_R	ROSE.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R317_R	ROSE.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R306_R	ROSE.X
152S01109	1	IND,FILM,0.6NH,950MA,01005	R316_R	ROSE.X
131S00030	1	CAP,CER,C0G,0.4PF,16V,01005	C317_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C304_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C314_R	ROSE.X
152S01109	1	IND,FILM,0.6NH,950MA,01005	R309_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C303_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C313_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C302_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C312_R	ROSE.X
152S00494	1	IND,FILM,0.8NH,900MA,01005	R307_R	ROSE.X
152S00494	1	IND,FILM,0.8NH,900MA,01005	R308_R	ROSE.X
131S0369	1	CAP,CER,C0G,0.5PF,16V,01005	C315_R	ROSE.X

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00497	1	IND,FILM,0.5NH,1000MA,01005	R305_R	ROSE.0
152S00497	1	IND,FILM,0.5NH,1000MA,01005	R317_R	ROSE.0
152S00498	1	IND,FILM,0.4NH,1000MA,01005	R306_R	ROSE.0
152S00492	1	IND,FILM,1.0NH,900MA,01005	R316_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C317_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C304_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C314_R	ROSE.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R309_R	ROSE.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R308_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C302_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C312_R	ROSE.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R307_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C303_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C313_R	ROSE.0
131S00030	1	CAP,CER,C0G,0.4PF,16V,01005	C315_R	ROSE.0

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00664	339S00665	ALT_PARTS	U_ROSE_R	MODULE,STRIDER,ES5.1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

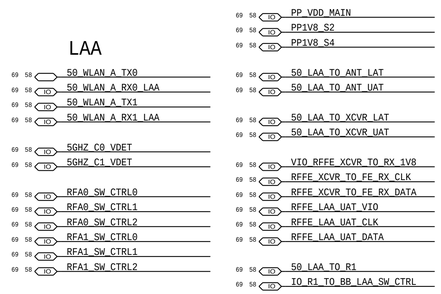
LAA_WIFI (GODFATHER)

LAST_MODIFICATION=Fri May 3 22:17:24 2019

PAGE	CSA	CONTENTS	SYNC	DATE
68	1	FEM MODULES		
69	2	FEM MODULES		05/08/2018

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00422	1	IND,FILM,1.5NH,700MA,01005	R362_W	WIFI.0
152S00498	1	IND,FILM,0.4NH,1000MA,01005	R363_W	WIFI.0
152S00498	1	IND,FILM,0.4NH,1000MA,01005	R372_W	WIFI.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R373_W	WIFI.0
131S0893	1	CAP,CER,C0G,0.2PF16V,01005	C361_W	WIFI.0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00419	1	IND,FILM,1.1NH,01005	R362_W	WIFI.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R363_W	WIFI.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R372_W	WIFI.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R373_W	WIFI.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C361_W	WIFI.X



SCHEMATIC APN: 951-08431

FEM MODULES

STUFF ONLY FOR VENDOR CONFIG

DOMAIN (E.P.S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	PP1V8_UAT_FEM_LNA, PP1V8_LAT_FEM_LNA, RFFE_*VIO, PP_1V8_VIO_LAA*

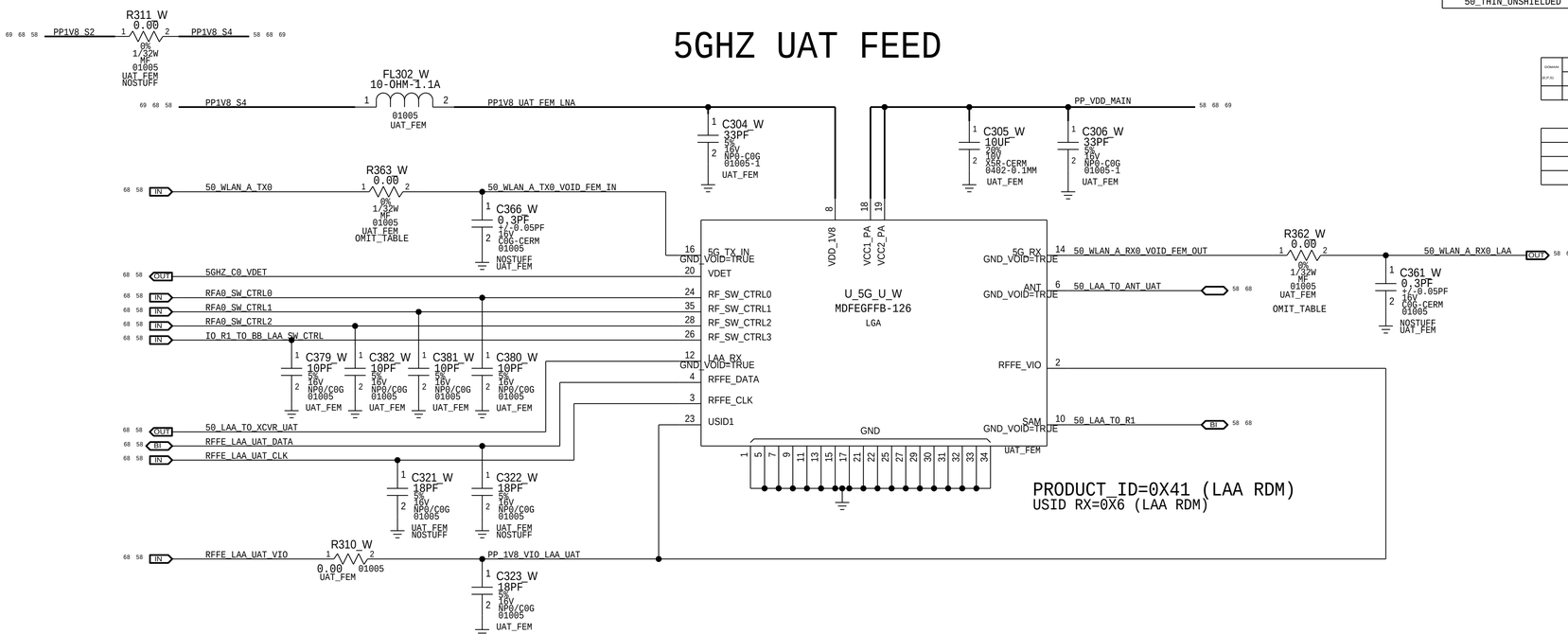
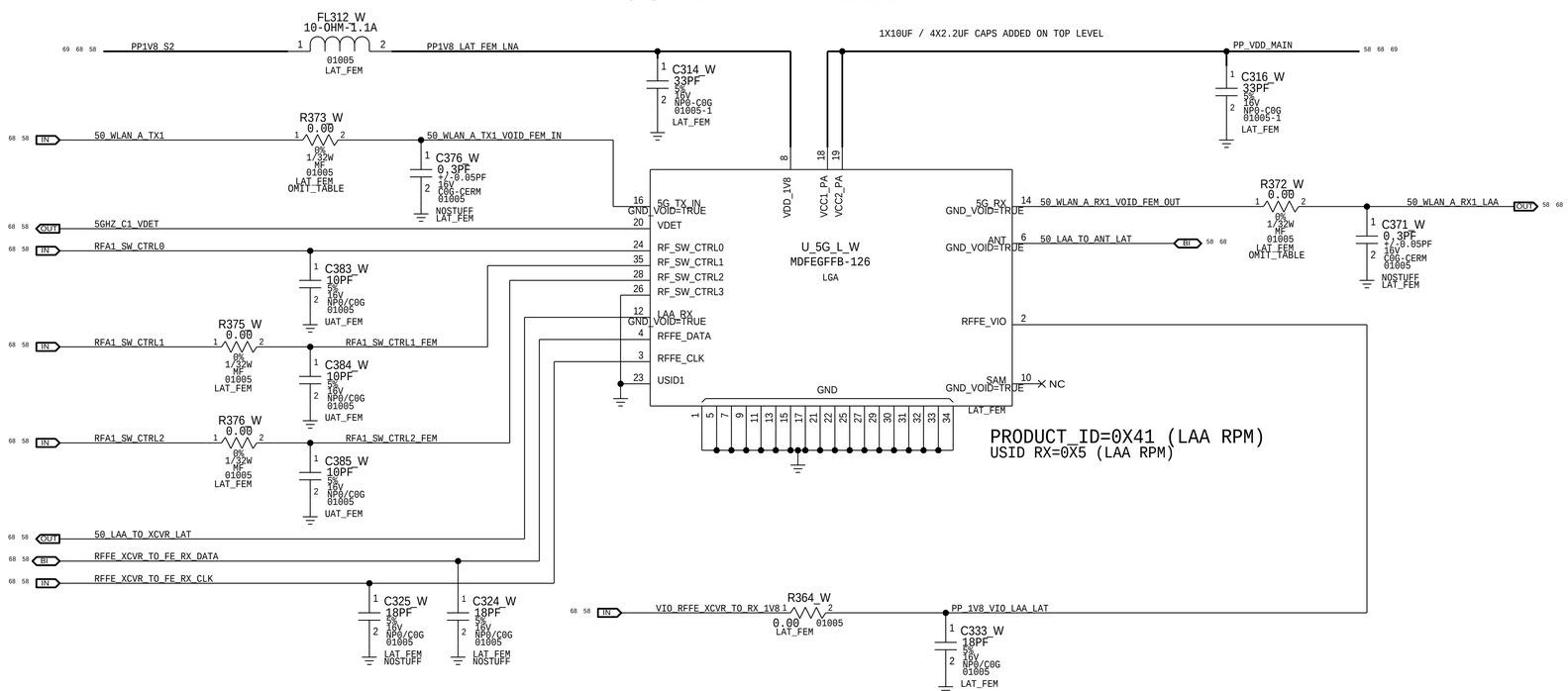
Table Modified Locally

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHAMFER
CLASS NAME	DIFF P/S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
WLAN_SHIELD		S A_DIELECTRIC_2X	RFA0_SW*, RFA1_SW*	?
RF_SHIELD		S A_DIELECTRIC_2X	*R1_TO_BB_LAA_SW*, 5GHZ_C*	?
50_THIN_UNSHIELDED		S A_DIELECTRIC_2X	50_LAA_TO_XCVR*	?

DOMAIN (E.P.S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_LAA_TO_XCVR* Table Modified Locally

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
WLAN_SHIELD	WLAN_SHIELD	DEFAULT
WLAN_SHIELD	GND	DEFAULT

5GHZ UAT FEED



5GHZ LAT FEED